VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD512M16XS54XX1V75 USER MANUAL

Version : B0

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Contents

VDIC-SDRAM

HIGH-SPEED 3.3V 32M×16bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

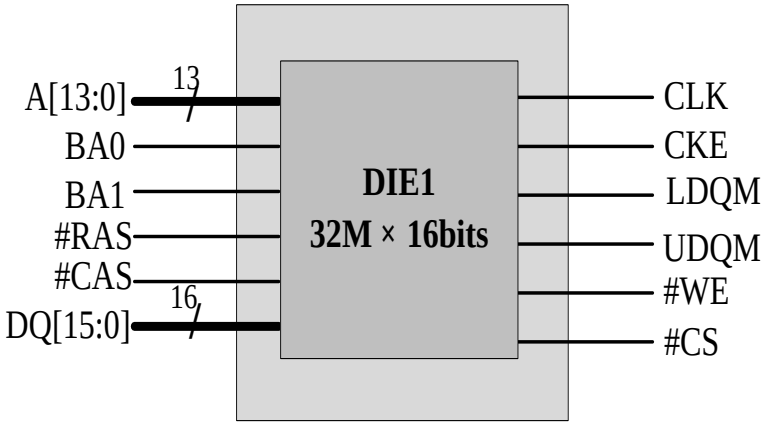
The VDSD512M16XS54XX1V75 is a 512M bits SDRAM, organized as 32M words×16 bits. The device has one die including 8M×16bits×4bank. All inputs and outputs are referred to the rising edge of the clock input. Allow the device to be useful for a variety of high bandwidth, high performance memory system applications. It is packaged in 54-pin SOP.

2 FEATURES

- Single 3.3V ±0.3V power supply
- Clock frequency:166,143,133MHz
- LVTTL interface
- Fully synchronous; all signals referenced to a positive clock edge
- Programmable burst length –(1,2,4,8,full page)
- Programmable burst sequence:Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency (2,3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 54-pin SOP

3 BLOCK DIAGRAM

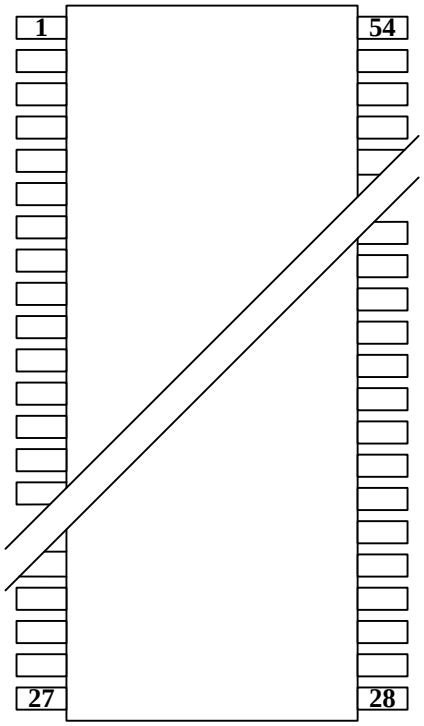
FIGURE 1: Signal link of Block Diagram



4 PIN DESCRIPTIONS

FIGURE 3: Pin Descriptions

Pin Id	Pin #		Pin Id
VDD	1	54	**VSS**
DQ0	2	53	**DQ15**
VDDQ	3	52	**VSSQ**
DQ1	4	51	**DQ14**
DQ2	5	50	**DQ13**
VSSQ	6	49	**VDDQ**
DQ3	7	48	**DQ12**
DQ4	8	47	**DQ11**
VDDQ	9	46	**VSSQ**
DQ5	10	45	**DQ10**
DQ6	11	44	**DQ9**
VSSQ	12	43	**VDDQ**
DQ7	13	42	**DQ8**
VDD	14	41	**VSS**
LDQM	15	40	**NC**
#WE	16	39	**UDQM**
#CAS	17	38	**CLK**
#RAS	18	37	**CKE**
#CS	19	36	**A12**
BA0	20	35	**A11**
BA1	21	34	**A9**
A10	22	33	**A8**
A0	23	32	**A7**
A1	24	31	**A6**
A2	25	30	**A5**
A3	26	29	**A4**
VDD	27	28	**VSS**



Name	Function
A0~A12	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0-DQ15	Data Input/ Output Ports. 16 bi-directional ports are used to read data from or write data into the SDRAM.
#CS	Chip select: #CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when #CS is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while#CS is HIGH. #CS provides for external bank selection on systems with multiple banks. #CS is considered part of the command code.
BA0,BA1	Bank address input(s): BA[1:0] defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
#RAS	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Write Enable Input. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
LDQM, HDQM	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. LDQM corresponds to DQ[7:0] and DQ[23:15], and UDQM corresponds to DQ[15:8] and DQ[31:24]. LDQM and UDQM are considered same state when referenced as DQM.

Name	Function
CLK	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
V_{DDQ}	DQ power: DQ power to the die for improved noise immunity.
V_{SSQ}	DQ ground: DQ ground to the die for improved noise immunity.
V_{DD}	Power supply: 3.3V ±0.3V.
V_{SS}	Ground
NC	No connect

5 ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}/ V_{DDQ}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to V_{DD} +0.5	V
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_{OPR}	-55~ +105	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

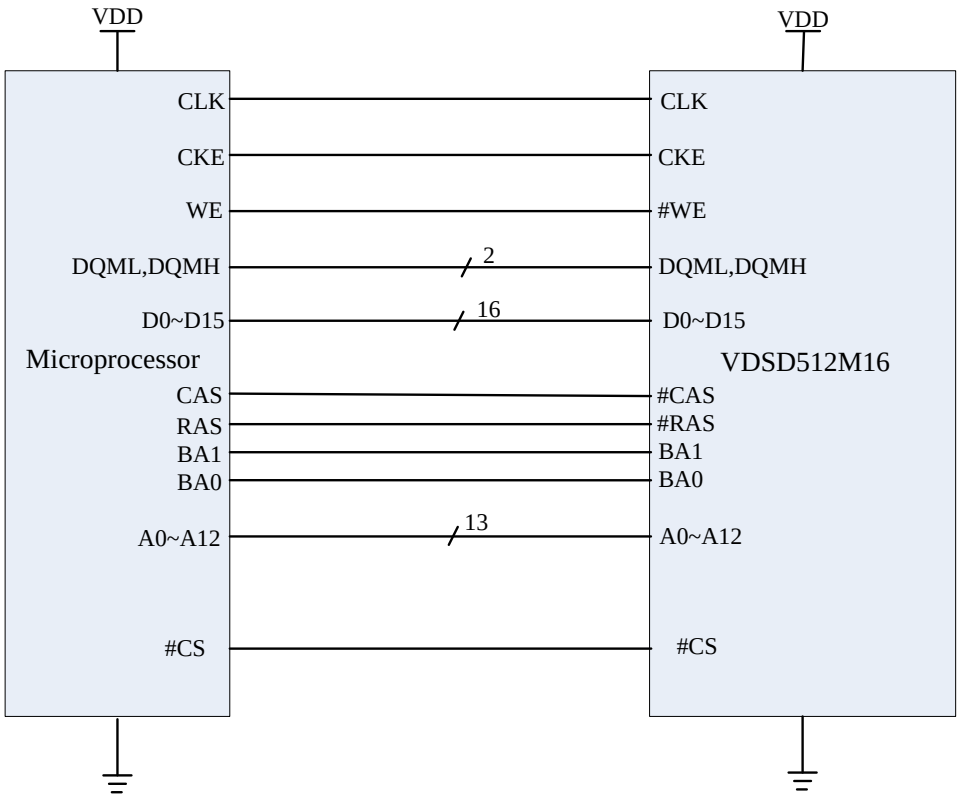
5.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	——	V_{DD}+0.3	V
	V_{IL}	-0.3	——	0.8	V

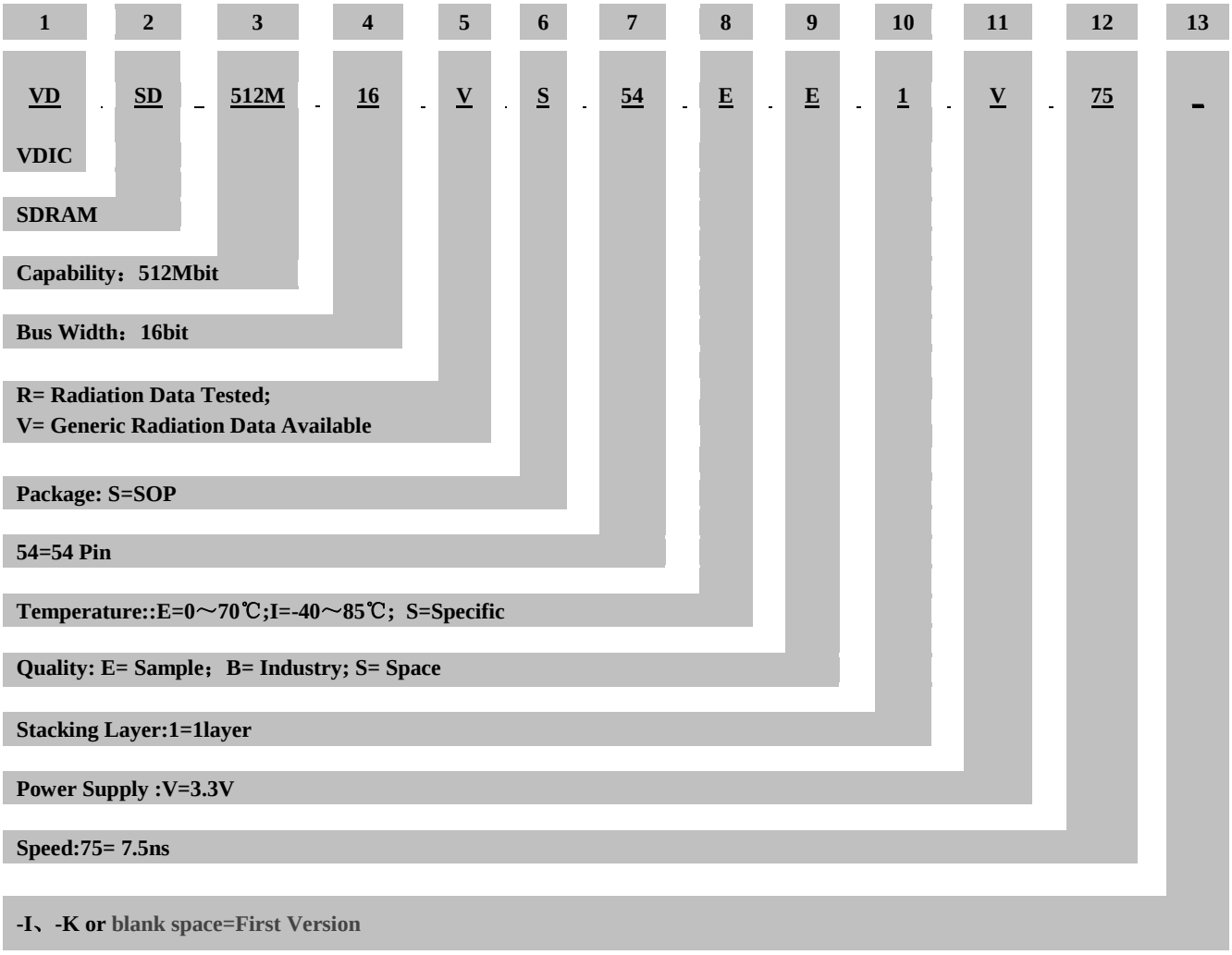
5.3 DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	I_{OL}=2mA	——	0.4	V

6 TYPICAL APPLICATION



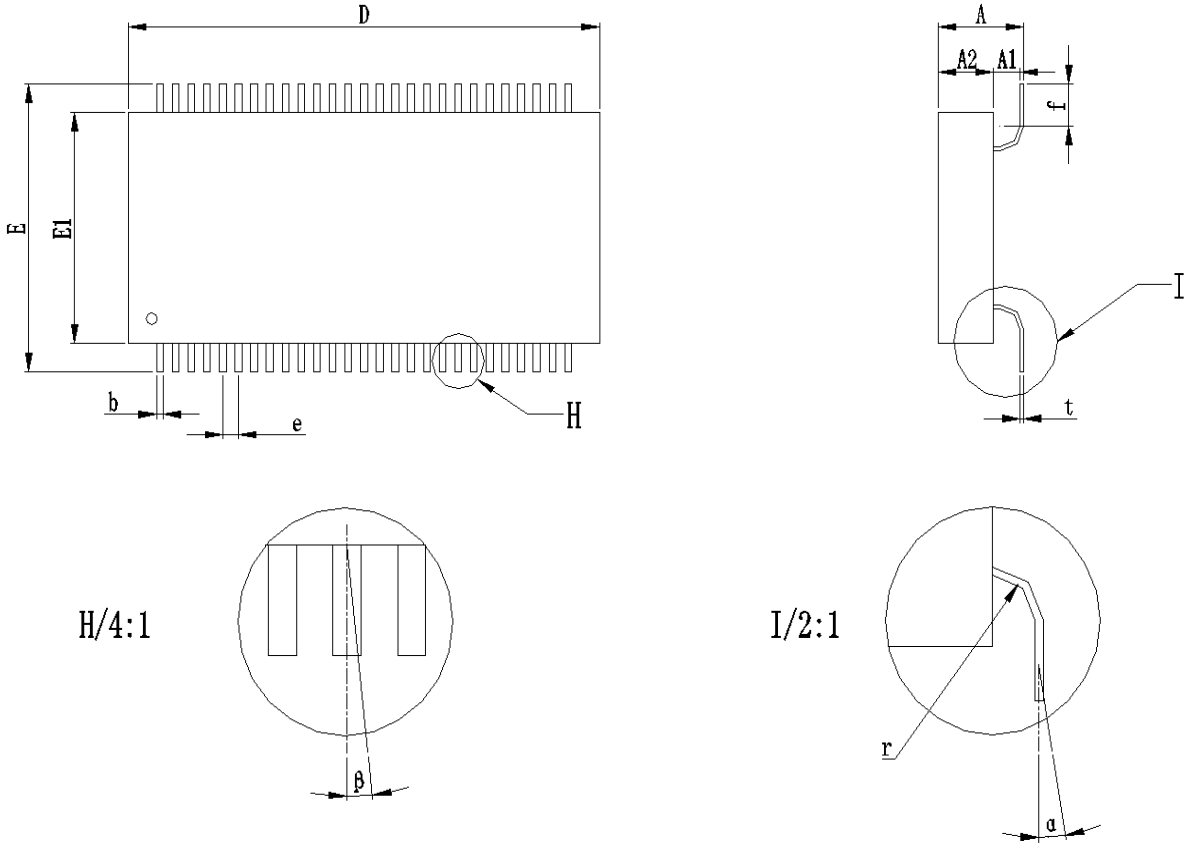
7 ORDERING INFORMATION



Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD512M16VS54EE1V75	512M	16	-	-	-	SOP54	0~+70
VDSD512M16VS54IB1V75	512M	16	-	-	-	SOP54	-40~+85
VDSD512M16RS54SS1V75	512M	16	>50	>80	1	SOP54	-55~+105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS



	Min	Max
A	3.70	4.40
A2	2.50	3.10
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.8	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE：1.U int：mm 2. A1= A - A2		

9 REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Aug 23,2016	Modified ORDERING INFORMATION
A3	Jan 9,2017	Modified the Truth Table
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov 10,2017	Add or reduce chapters
B0	Apr 13,2018	Modified DC characteristics table