# VDIC SYNCHRONOUS DYNAMIC SDRAM

# VDSD4G16XS62XX8V75 USER MANUAL

**Version ：B0**

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# Contents

# VDIC-SDRAM

## HIGH-SPEED 3.3V 256M×16bit

## SYNCHRONOUS DYNAMIC SDRAM

## 1 DESCRIPTION

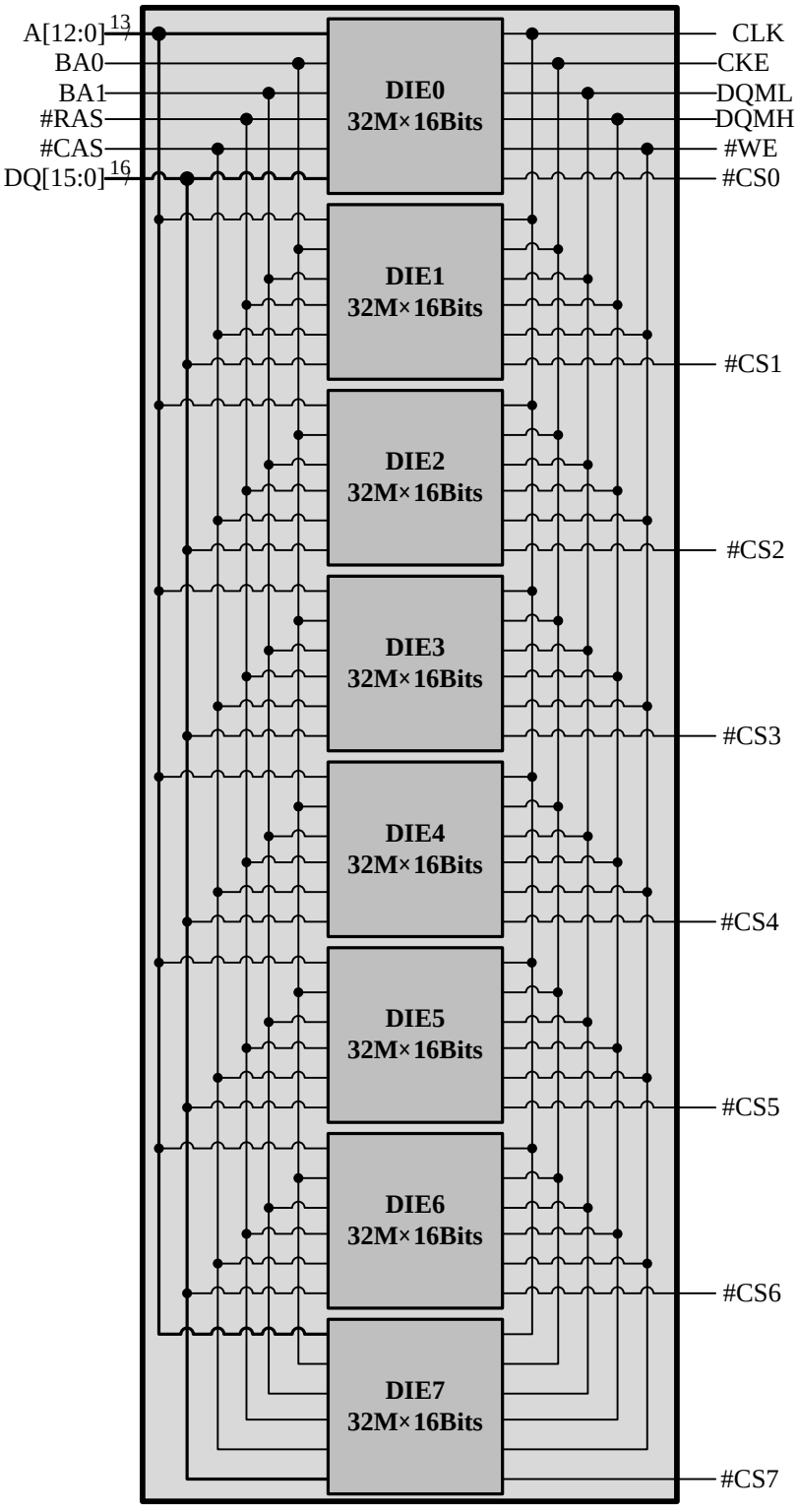
The VDSD4G16XS62XX8V75 is a 4,096M bits SDRAM, organized as 256M words×16bits. The device has 8 dies, every die include 8,388,608 words×16bits×4bank, and a chip select individual. All inputs and outputs are referred to the rising edge of the clock input. Allow the device to be useful for a variety of high bandwidth, high performance memory system applications. It is packaged in 62-pin SOP.

## 2 FEATURES

- Single 3.3V ±0.3V power supply
- Clock frequency:166,143,133MHz
- LVTTL interface
- Fully synchronous; all signals referenced to a positive clock edge
- Programmable burst length –(1,2,4,8,full page)
- Programmable burst sequence:Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency (2,3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 62-pin SOP

# 3 BLOCK DIAGRAM

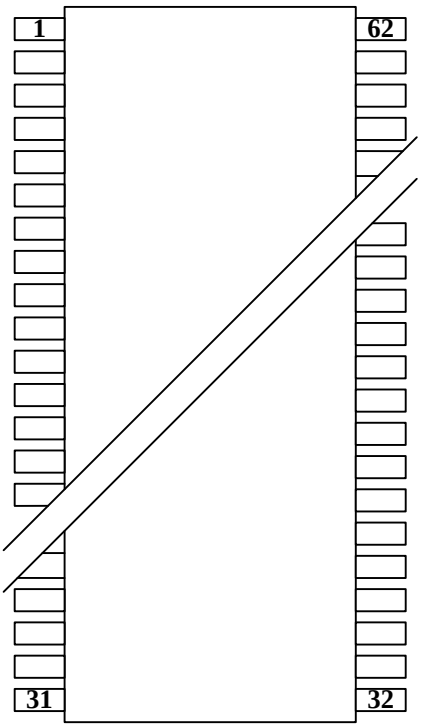
FIGURE 1: Signal link of Block Diagram



# 4 PIN DESCRIPTIONS

**FIGURE 3: Pin Descriptions**

| Pin Id | Pin # | | Pin Id |
|---|---|---|---|
| **#CS4** | 1 | 62 | **NC** |
| **#CS3** | 2 | 61 | **NC** |
| **VDD** | 3 | 60 | **VSS** |
| **DQ0** | 4 | 59 | **DQ15** |
| **VDDQ** | 5 | 58 | **VSSQ** |
| **DQ1** | 6 | 57 | **DQ14** |
| **DQ2** | 7 | 56 | **DQ13** |
| **VSSQ** | 8 | 55 | **VDDQ** |
| **DQ3** | 9 | 54 | **DQ12** |
| **DQ4** | 10 | 53 | **DQ11** |
| **VDDQ** | 11 | 52 | **VSSQ** |
| **DQ5** | 12 | 51 | **DQ10** |
| **DQ6** | 13 | 50 | **DQ9** |
| **VSSQ** | 14 | 49 | **VDDQ** |
| **DQ7** | 15 | 48 | **DQ8** |
| **VDD** | 16 | 47 | **VSS** |
| **LDQM** | 17 | 46 | **#CS7** |
| **#WE** | 18 | 45 | **UDQM** |
| **#CAS** | 19 | 44 | **CLK** |
| **#RAS** | 20 | 43 | **CKE** |
| **#CS0** | 21 | 42 | **A12** |
| **BA0** | 22 | 41 | **A11** |
| **BA1** | 23 | 40 | **A9** |
| **A10** | 24 | 39 | **A8** |
| **A0** | 25 | 38 | **A7** |
| **A1** | 26 | 37 | **A6** |
| **A2** | 27 | 36 | **A5** |
| **A3** | 28 | 35 | **A4** |
| **VDD** | 29 | 34 | **VSS** |
| **#CS1** | 30 | 33 | **#CS5** |
| **#CS2** | 31 | 32 | **#CS6** |




| Name | Function |
|---|---|
| A0~A12 | Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a |

| Name | Function |
|---|---|
| | LOAD MODE REGISTER command. |
| DQ0-DQ15 | Data Input/ Output Ports. 16 bi-directional ports are used to read data from or write data into the SDRAM. |
| #CS0 (Die0) | Chip select: #CSn enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when #CSn is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while #CS is HIGH. #CSn provides for external bank selection on systems with multiple banks. #CSn is considered part of the command code. |
| #CS1 (Die1) | |
| #CS2 (Die2) | |
| #CS3 (Die3) | |
| #CS4 (Die4) | |
| #CS5 (Die5) | |
| #CS6 (Die6) | |
| #CS7 (Die7) | |
| BA0,BA1 | Bank address input(s): BA[1:0] defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. |
| #RAS | Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge. |
| #CAS | Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access. |
| #WE | Write Enable Input. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active. |
| DQML, DQMH | Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a |

| Name | Function |
|---|---|
| | High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ[7:0], and DQMH corresponds to DQ[15:8]. DQML and DQMH are considered same state when referenced as DQM. |
| CLK | Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers. |
| CKE | Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH. |
| $V_{DDQ}$ | DQ power: DQ power to the die for improved noise immunity. |
| $V_{SSQ}$ | DQ ground: DQ ground to the die for improved noise immunity. |
| $V_{DD}$ | Power supply: +3.3V ±0.3V. |
| $V_{SS}$ | Ground |
| NC | No connect |

# 5 ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 5.1 Absolute Maximum Ratings

| Characteristics | Symbol | Maximum ratings | Unit |
|---|---|---|---|
| Voltage on $V_{DD}$ supply relative to Vss | $V_{DD}$/ $V_{DDQ}$ | -0.5 to +4.6 | V |
| Voltage on any pin relative to Vss | $V_{IN}$ | -0.5 to $V_{DD}$ +0.5 | V |
| Power Dissipation | $P_D$ | 1.2 | W |
| Operating Temperature Range | $T_{OPR}$ | -55~ +105 | ℃ |
| Storage Temperature Range | $T_{STG}$ | -65 to +150 | ℃ |

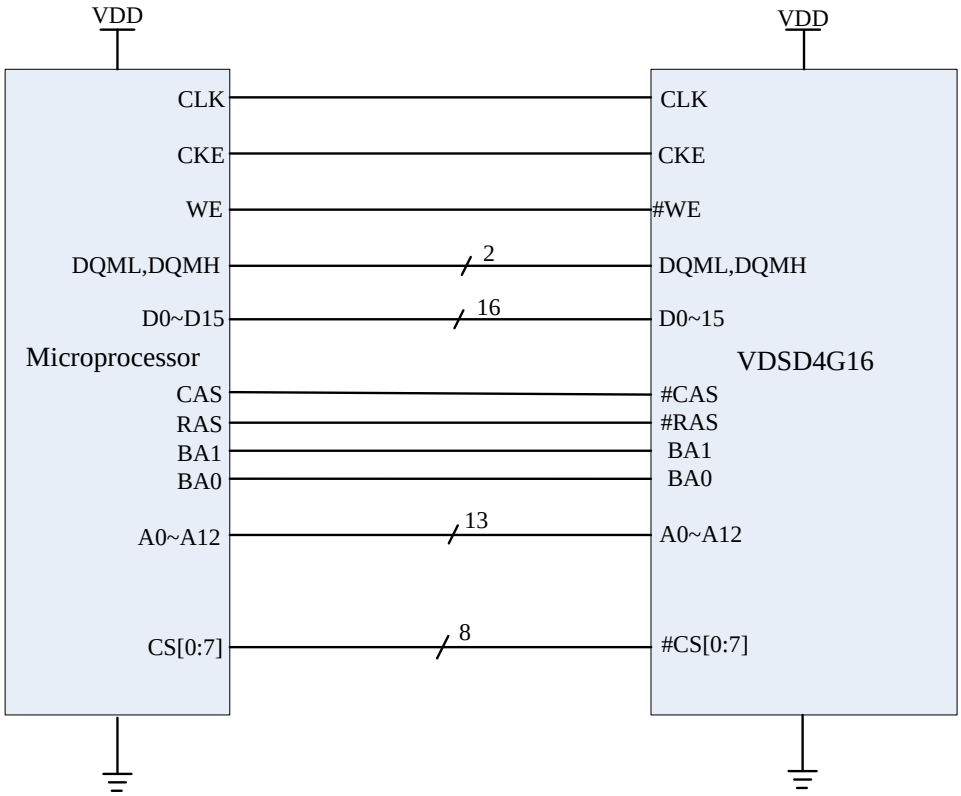
## 5.2 Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V |
| Input voltage | $V_{IH}$ | 2.0 | —— | $V_{DD}$+0.3 | V |
| | $V_{IL}$ | -0.3 | —— | 0.8 | V |

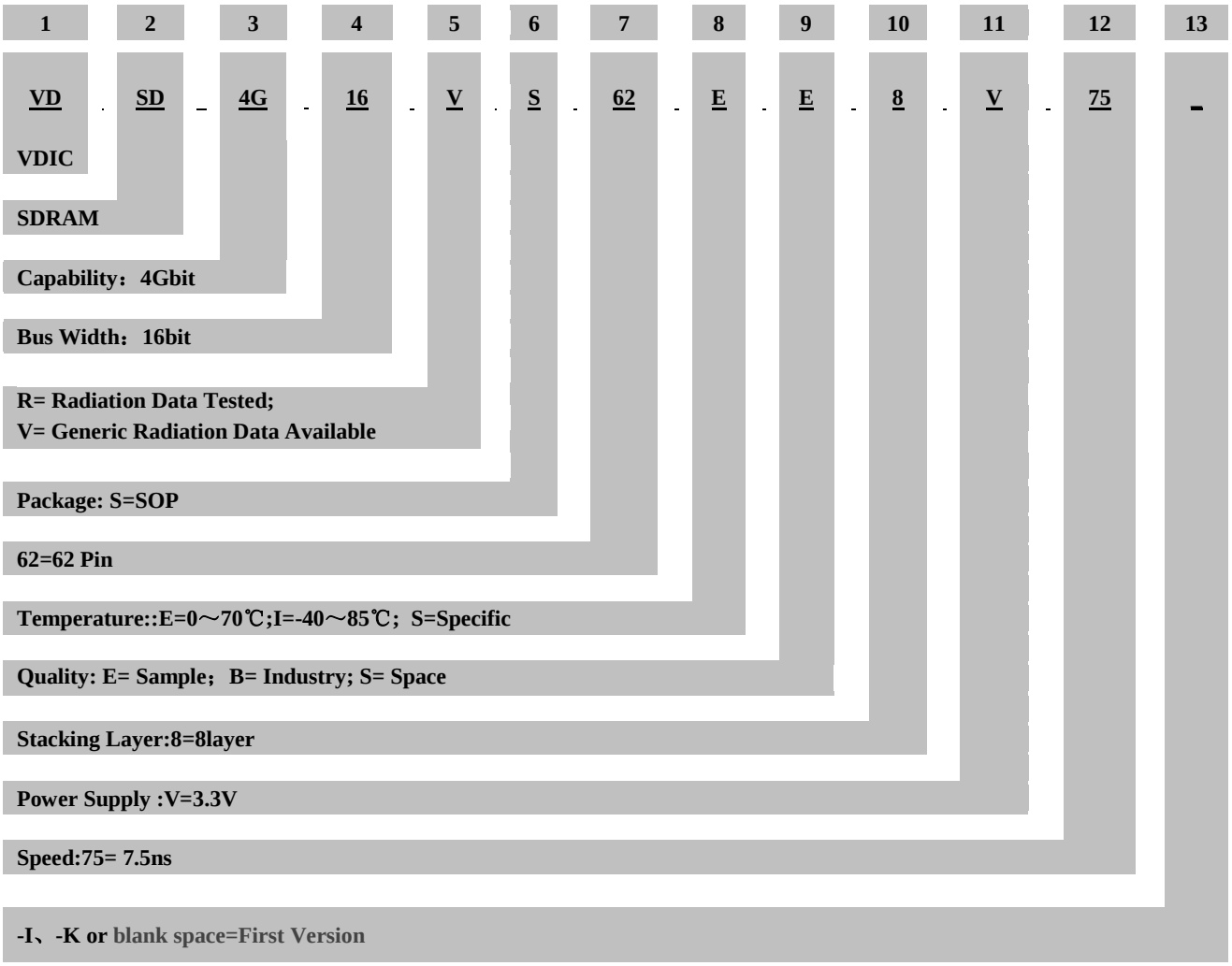
## 5.3 DC Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Output High Voltage Level | $V_{OH}$ | $I_{OH}$=-2mA | 2.4 | —— | V |
| Output Low Voltage Level | $V_{OL}$ | $I_{OL}$=2mA | —— | 0.4 | V |

# 6 TYPICAL APPLICATION



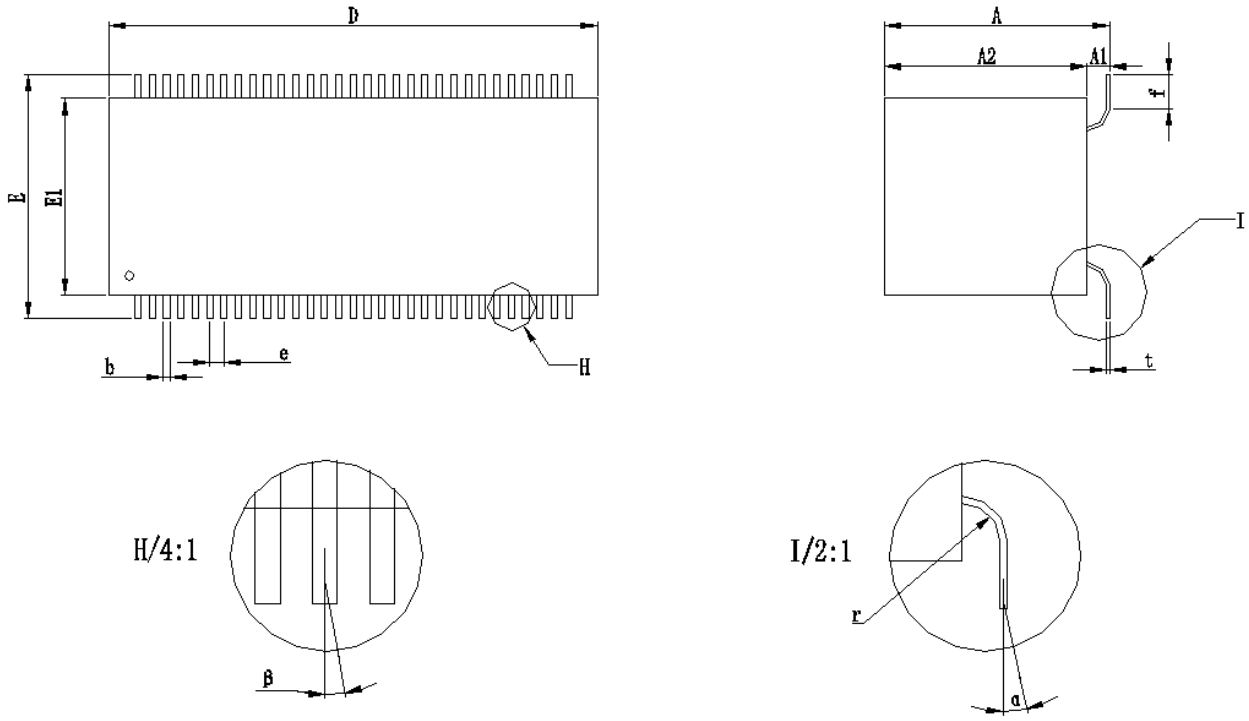
# 7 ORDERING INFORMATION




| Part Number | Capacity (bit) | Bus Width (bit) | Radiation | | | Packaging | Temperature ( ℃ ) |
|---|---|---|---|---|---|---|---|
| | | | TID[1] | SEL[2] | SEU[3] | | |
| VDSD4G16VS62EE8V75 | 4G | 16 | - | - | - | SOP62 | 0~+70 |
| VDSD4G16VS62IB8V75 | 4G | 16 | - | - | - | SOP62 | -40~+85 |
| VDSD4G16RS62SS8V75 | 4G | 16 | >50 | >80 | 1 | SOP62 | -55~+105 |

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

# 8 PACKAGE DIMENSIONS




| | Min | Max |
|---|---|---|
| A | 12.30 | 12.80 |
| A2 | 11.10 | 11.50 |
| D | 27.00 | 27.40 |
| E | 13.40 | 13.80 |
| E1 | 10.80 | 11.20 |
| f | 2.00 | |
| b | 0.35 | |
| e | 0.80 | |
| r | 1.00 | |
| t | 0.20 | |
| α | ≤3° | |
| β | ≤3° | |
| NOTE：1.U int：mm<br>2. A1= A - A2 | | |

# 9 REVISION HISTORY

| Revision | Date | Description of Change |
|---|---|---|
| A0 | Nov 3,2015 | First Created |
| A1 | Mar 14,2016 | Modified PIN DESCRIPTIONS |
| A2 | Aug 23,2016 | Modified ORDERING INFORMATION |
| A3 | Jan 9,2017 | Modified the Truth Table |
| A4 | Oct.25,2017 | Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd |
| A5 | Nov 10,2017 | Add or reduce chapters |
| B0 | Apr 11,2018 | Modified DC characteristics table |