VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD3G48XQ114XX6V75 USER MANUAL

Version : B0

Contents

VDIC-SDRAM

HIGH-SPEED 3.3V 64M×48bit

## SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION
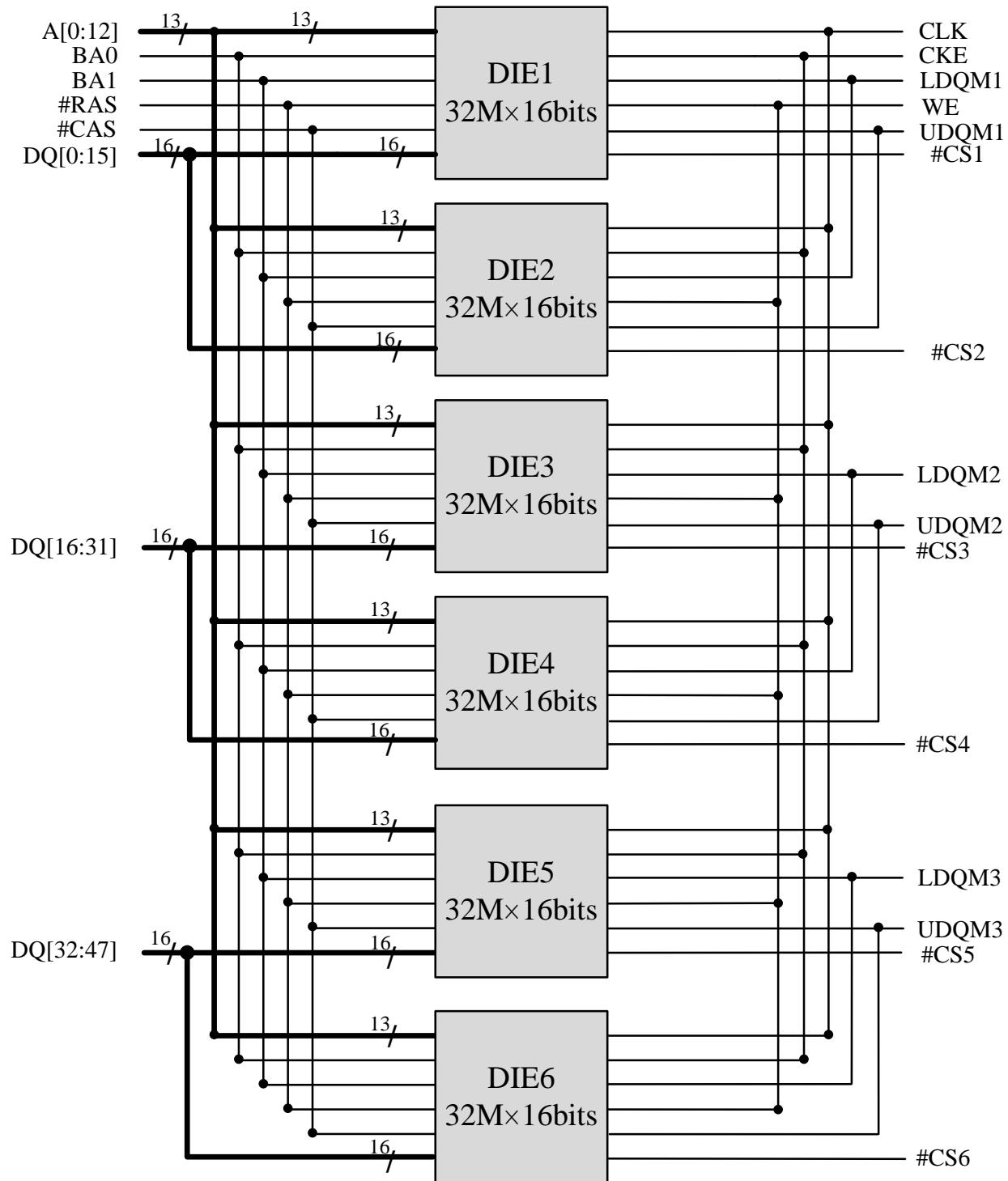
The VDSD3G48XQ114XX6V75 is a 3,072M bits SDRAM, organized as 64M words×48 bits . The device has six dies, every die include8,388,608 words×16 bits×4 bank, and per chip select is individual. All inputs and outputs are referred to the rising edge of the clock input. Allow the device to be useful for a variety of high bandwidth, high performance memory system applications. It is packaged in 114-pin QFP.

2 FEATURES

- Single 3.3V ±0.3V power supply
- Clock frequency:166,143,133MHz
- LVTTL interface
- Fully synchronous; all signals   referenced to a positive clock edge
- Programmable burst length–(1,2,4,8,full page)
- Programmable burst sequence:Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency(2,3clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 114-pin QFP

3 BLOCK DIAGRAM

FIGURE 1: Signal link of Block Diagram

4 PIN DESCRIPTIONS

FIGURE 3: Pin Descritions

| Pin Id	Pin #		Pin Id
VCC	1	114	VCCQ
VSS	2	113	VSSQ
D47	3	112	NC
D31	4	111	CKE
D15	5	110	#WE
NC	6	109	A12
#CS6	7	108	A11
#CS4	8	107	A10
VSSQ	9	106	A9
VCCQ	10	105	VSSQ
#CS2	11	104	VCCQ
NC	12	103	A8
NC	13	102	A7
LDQM1	14	101	A6
LDQM2	15	100	A5
LDQM3	16	99	A4
D46	17	98	A3
D30	18	97	A2
D14	19	96	VSS
D45	20	95	VCC
D29	21	94	VCC
D13	22	93	VSS
D44	23	92	A1
D28	24	91	A0
D12	25	90	BA1
D43	26	89	BA0
D27	27	88	#RAS
VCCQ	28	87	VSSQ
VSSQ	29	86	VCCQ
D11	30	85	#CAS
D42	31	84	NC
D26	32	83	#CS5
D10	33	82	#CS3
D41	34	81	#CS1
D25	35	80	CLK
VSS	36	79	NC
VCC	37	78	UDQM3
VCC	38	77	UDQM2
VSS	39	76	UDQM1
D9	40	75	D35
D40	41	74	D19
D24	42	73	D3
D8	43	72	D34
D39	44	71	D18
D23	45	70	D2
D7	46	69	D33
VCCQ	47	68	VCCQ
VSSQ	48	67	VSSQ
D38	49	66	D17
D22	50	65	D1
D6	51	64	D32
D37	52	63	D16
D21	53	62	D0
D5	54	61	D4
D36	55	60	D20
VSS	56	59	VSS
VCC	57	58	VCC
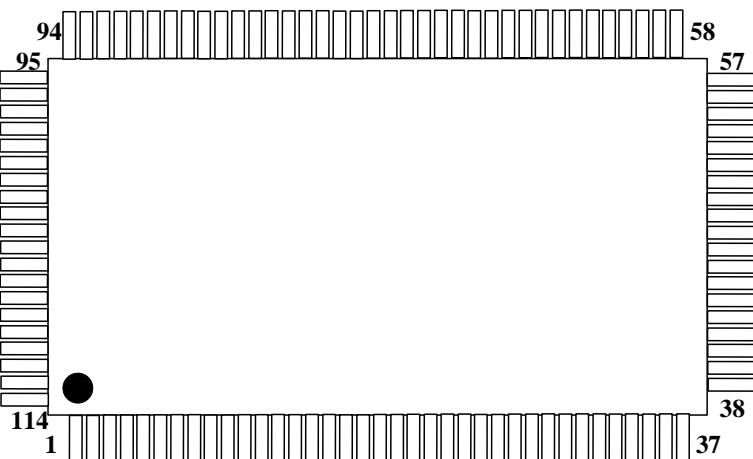
Table 1 Pin Description

Name	Function
A0~A12	Address Inputs: A0-A12 are sampled during the ACTIVE command (row-address A0-A12) and READ/WRITE command (column address A0-A9, with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0-DQ47	Data on the Data Bus is latched on DQ pins during Write commands, and buffered for output after Read commands.
#CS0 (Die1) #CS1 (Die2) #CS2 (Die3) #CS3 (Die4) #CS4 (Die5) #CS5 (Die6)	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is LOW, and disabled with $\overline{CS}$ is HIGH. The device remains in the previous state when $\overline{CS}$ is HIGH.
BA0,BA1	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
#RAS	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
#CAS	$\overline{CAS}$, in conjunction with the $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" for details on device commands.
#WE	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
DQML1 DQML2 DQML3	DQML and DQMH control the lower and upper bytes of the I/O buffers. In read DQMH mode, DQML and DQMH control the output buffer. When DQML or DQMH is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the

Name	Function
DQMH1	HIGH impedance state when DQML/DQMH is HIGH. This function corresponds to OE in conventional DRAMs. In write mode, DQML and DQMH control the input buffer. When DQML or DQMH is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When DQML or DQMH is HIGH, input data is masked and cannot be written to the device.
DQMH2	
DQMH3	
CLK	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
CKE	The CKE input determines whether the CLK input is enabled. The next rising edge of the CLK signal will be valid when is CKE HIGH and invalid when LOW. When CKE is LOW, the device will be in either power-down mode, clock suspend mode, or self refresh mode. CKE is an asynchronous input.
V_{CC}	V_{CC} is the device internal power supply.
V_{CCQ}	V_{CCQ} is the output buffer power supply.
V_{SS}	V_{SS} is the device internal ground.
V_{SSQ}	V_{SSQ} is the output buffer ground.
NC	No connect

5 ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}/ V_{CCQ}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to V_{CC} +0.5	V
Power Dissipation	P_D	3.0	W
Operating Temperature Range	T_{OPR}	-55~ +105	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2   Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	——	V_{CC}+0.3	V
	V_{IL}	-0.3	——	0.8	V

5.3 DC Electrical Characteristics

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	I_{OL}=2mA	——	0.4	V

6 TYPICAL APPLICATION
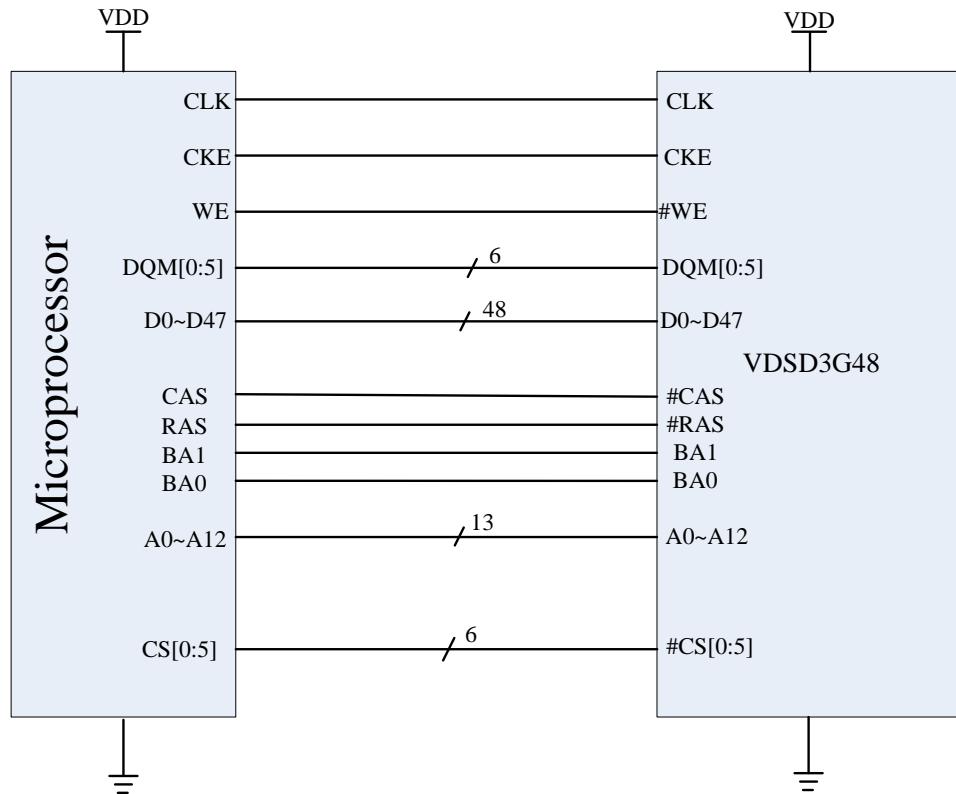
Figure 1 Typical application

7　ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13

| VD | SD | 3G | 48 | V | Q | 114 | E | E | 6 | V | 75 | _ |

VDIC

SDRAM

Capability：3G bit

Bus Width：48bit

R= Radiation Data Tested;
V= Generic Radiation Data Available

Package: Q=QFP

114=114 Pin

Temperature::E=0～70℃;I=-40～85℃;S=Specific

Quality: E= Sample；B= Industry; S= Space

Stacking Layer:6=6layer

Power Supply :V=3.3V

Speed:75= 7.5ns

-I、-K or blank space=First Version
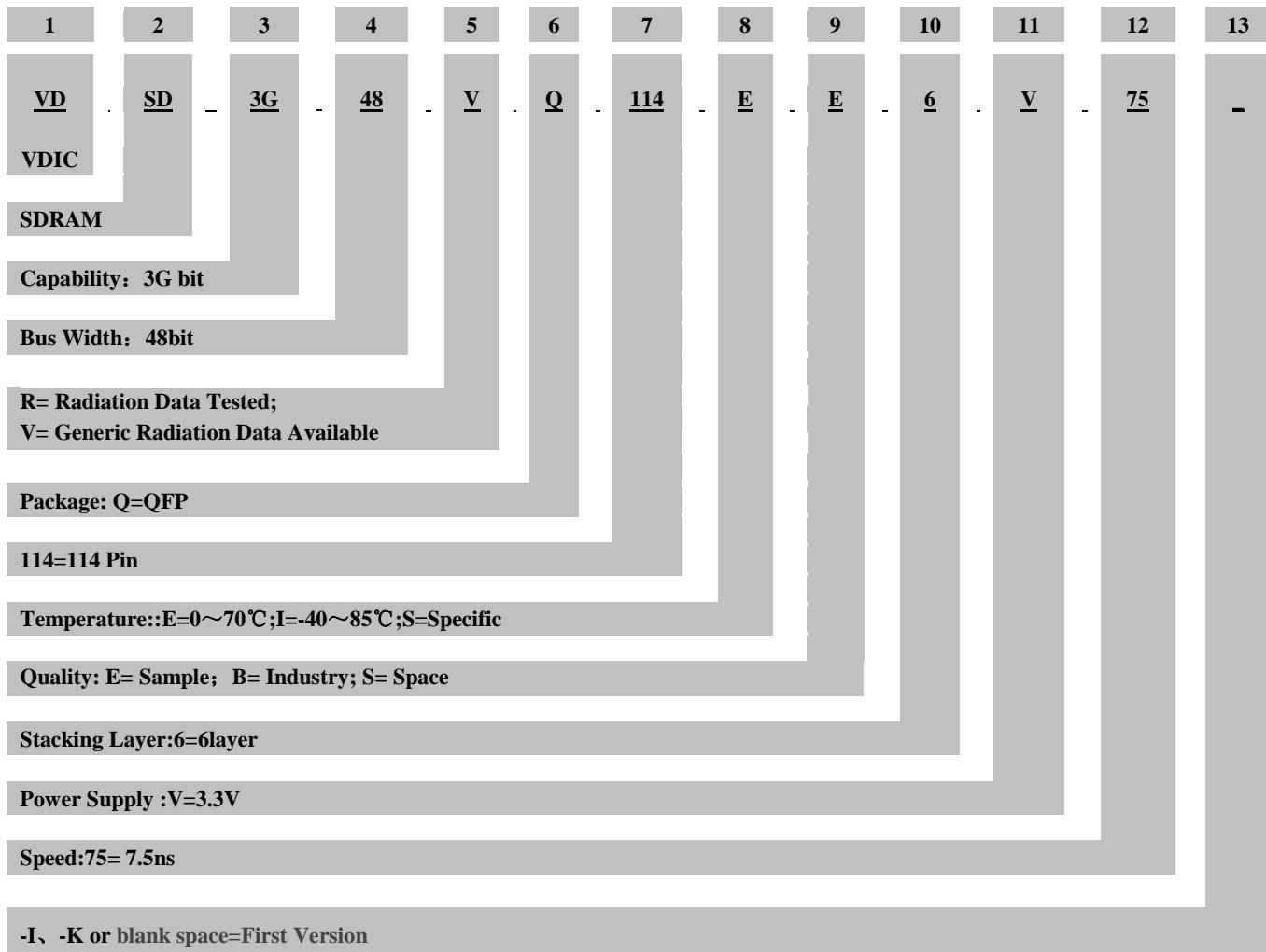
table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD3G48VQ114EE6V75	3G	48	-	-	-	QFP114	0 ～ + 70
VDSD3G48VQ114IB6V75	3G	48	-	-	-	QFP 114	-40 ～ + 85
VDSD3G48RQ114SS6V75	3G	48	>50	>80	1	QFP 114	-55 ～ + 105

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[1] TID: Total Dose （Krads(Si)）
[2] SEL: LET Threshold （Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS
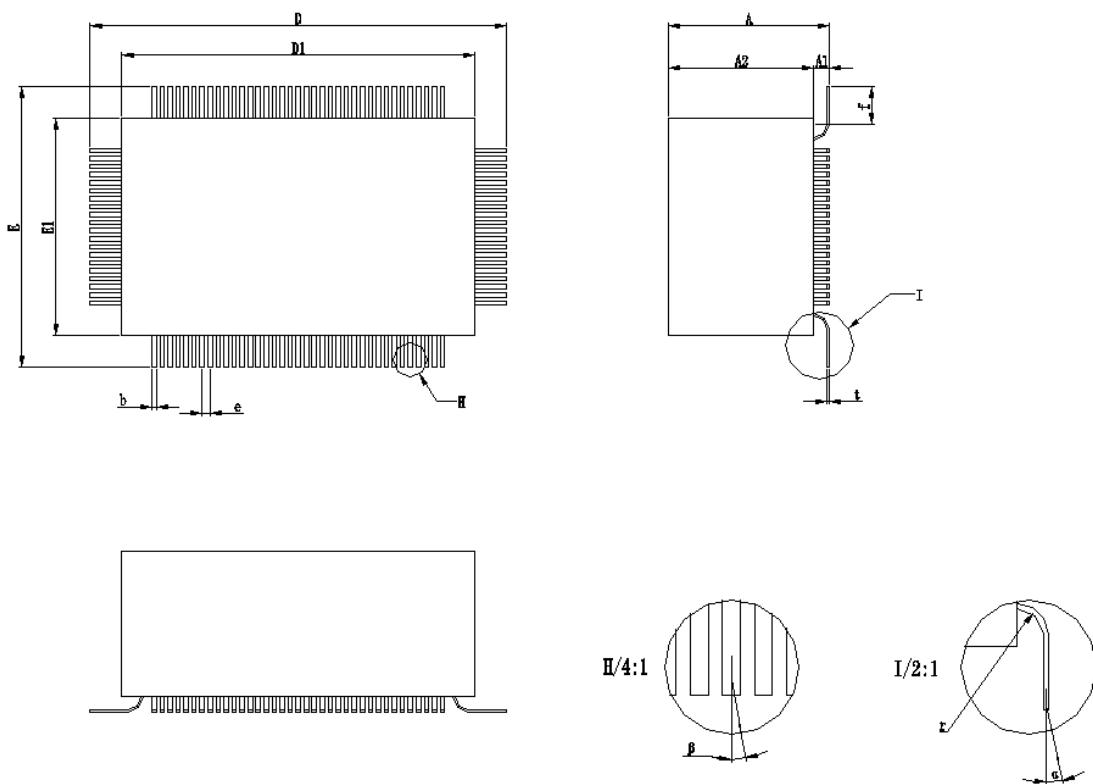
Table 6 Package dimensions

	Min	Max
A	12.10	13.20
A2	10.90	11.80
D	32.80	33.20
D1	27.80	28.20
E	21.80	22.40
E1	17.00	17.40
f	3.00	
b	0.35	
e	0.635	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	

NOTE：1.U int：mm
2. A1= A - A2

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Aug 23,2016	Modified ORDERING INFORMATION
A3	Jan 9,2017	Modified the Truth Table
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov 10,2017	Add or reduce chapters
B0	Mar 3,2018	Modified DC characteristics table