VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD2G40XS70XX5V75 USER MANUAL

Version : A5

Document NO.：ORBITA/SIP-VDSD2G40XS70XX5V75-USM-01
Zhuhai Orbita Aerospace Science & Technology Co.，Ltd.
Add: Orbita Tech Park，NO.1 Baisha Road，Tangjia Dong ` an，
Zhuhai，*Guangdong*，China 519080
Tel: +86-756-3391979　Fax: +86-756-3391980

Contents

VDIC-SDRAM

HIGH-SPEED 3.3V 64M×40bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

The VDSD2G40XS70XX5V75 is a 2.56G bits SDRAM, organized as 64M ×40bits. The device has five dies, every die include 134,217,728-bits, and a chip select individual. All inputs and outputs are referred to the rising edge of the clock input. It is has the ability to synchronously burst dadt at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide percharge time and the capability to randomly change column addresses on each clock cycle during burst access. It is packaged in 70-pin SOP.

2 FEATURES

- Single 3.3V ±0.3V power supply
- LVTTL interface
- Fully synchronous; all signals referenced to a positive clock edge
- Programmable burst length–(1,2,4,8,ful page)
- Programmable burst sequence:Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency (2,3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 70-pin SOP

3 BLOCK DIAGRAM

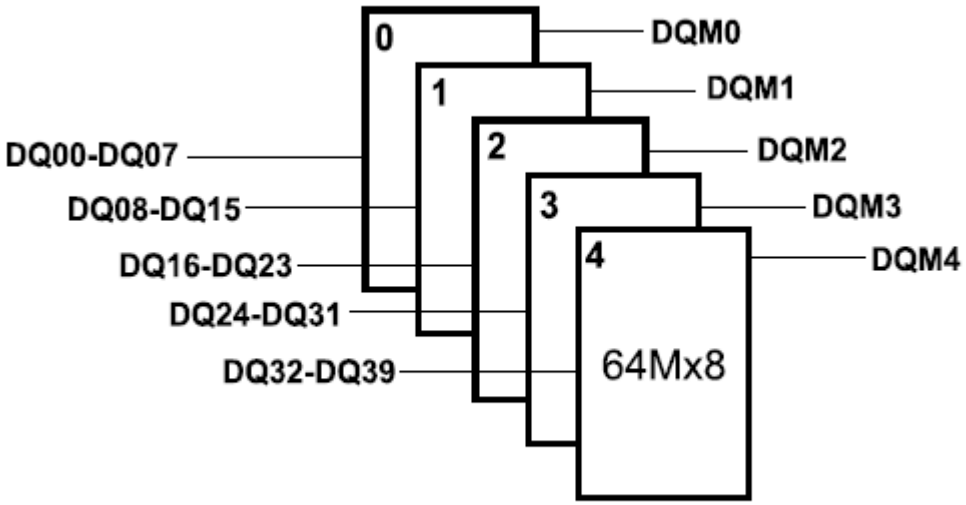
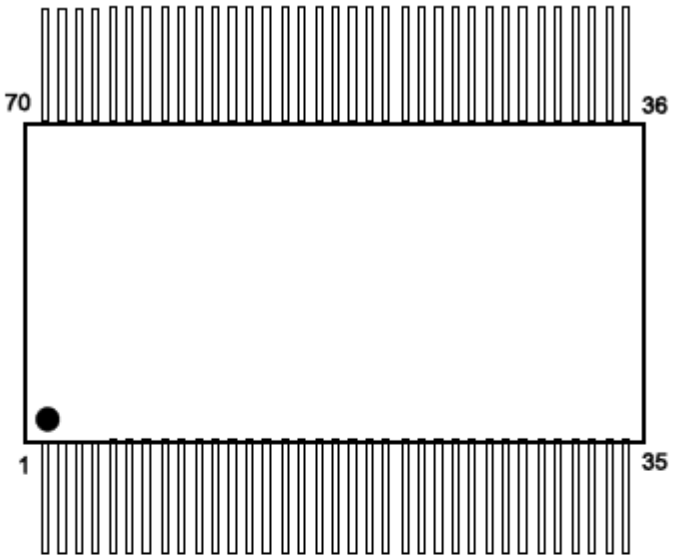


Figure 1 Block diagram

4 PIN DESCRIPTIONS



1	VDD	15	DQ26	29	A0	43	CKE	57	DQ21
2	DQ00	16	DQ34	30	A1	44	CLK	58	DQ29
3	DQ08	17	DQ03	31	A2	45	DQM0	59	DQ37
4	DQ16	18	DQ11	32	A3	46	DQM1	60	DQ06
5	DQ24	19	DQ19	33	A4	47	DQM2	61	DQ14
6	DQ32	20	DQ27	34	A5	48	DQM3	62	DQ22
7	DQ01	21	DQ35	35	VDD	49	DQM4	63	DQ30
8	DQ09	22	#WE	36	VSS	50	DQ4	64	DQ38
9	DQ17	23	#CAS	37	A6	51	DQ12	65	DQ07
10	DQ25	24	#RAS	38	A7	52	DQ20	66	DQ15
11	DQ33	25	#CS	39	A8	53	DQ28	67	DQ23
12	DQ02	26	BA0	40	A9	54	DQ36	68	DQ31
13	DQ10	27	BA1	41	A11	55	DQ05	69	DQ39
14	DQ18	28	A10	42	A12	56	DQ13	70	VSS

Figure 2 Pin configuration

Table 1 Pin description

Symbol	Type	Description
A0~A12	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0-DQ40	I/O	Data Input/ Output Ports.
#CS	Input	Chip select:#CSn enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when #CSn is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while #CSn is HIGH. #CSn provides for external bank selection on systems with multiple banks. #CSn is considered part of the command code.
BA [1:0]	Input	Bank address input(s): BA[1:0] defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
#RAS	Input	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Input	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Input	Write Enable Input. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
DQM	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle.

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
V_{DD}	Supply	Power supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground
NC	-	These should be left unconnected.

5 ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}/ V_{DDQ}	-1.0 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-1.0 to V_{DD} +0.5	V
Power Dissipation	P_D	2.0	W
Operating Temperature Range	T_{OPR}	-55~ +105	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	——	V_{DD}+0.3	V
	V_{IL}	-0.3	——	+0.8	V

5.3 DC Characteristics

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	I_{OL}=2mA	——	0.4	V

6 TYPICAL APPLICATION

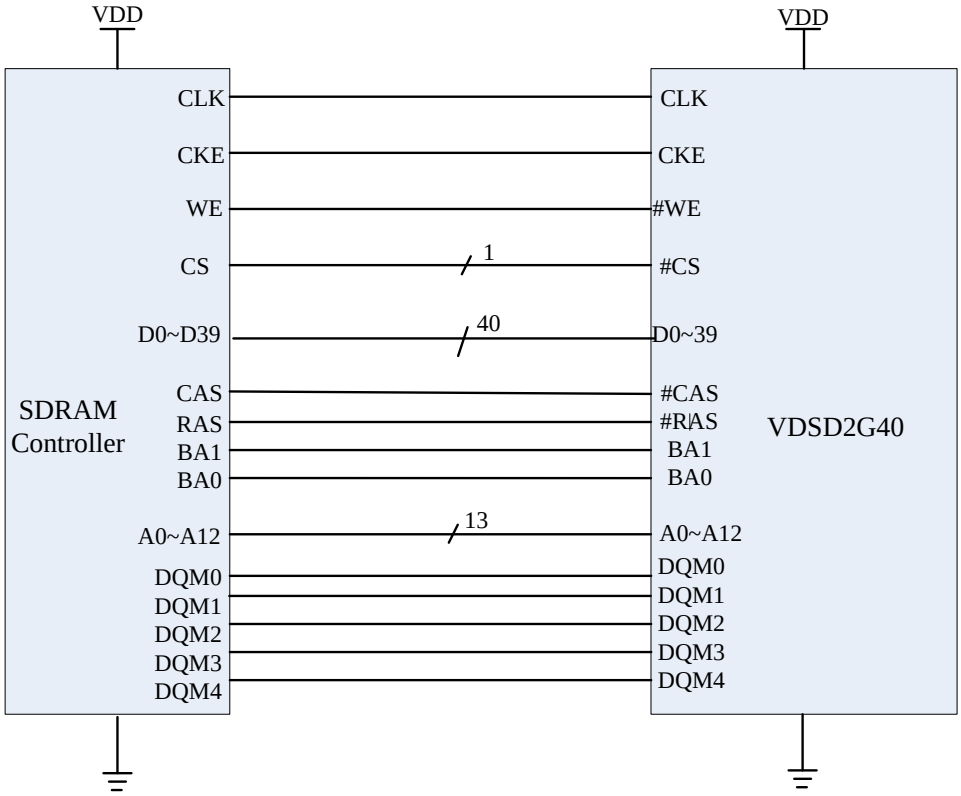


Figure 3 Typical application

7 ORDERING INFORMATION

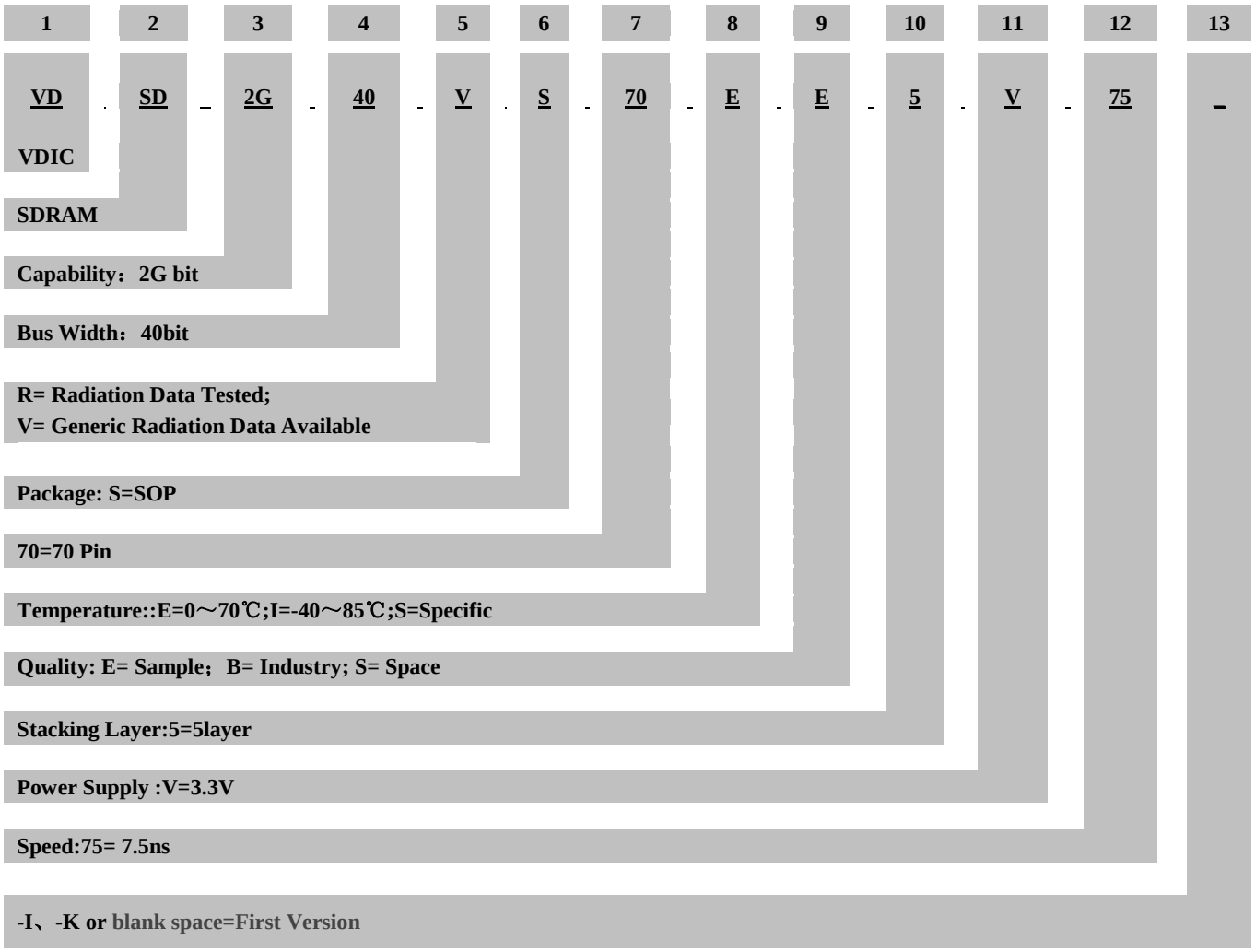
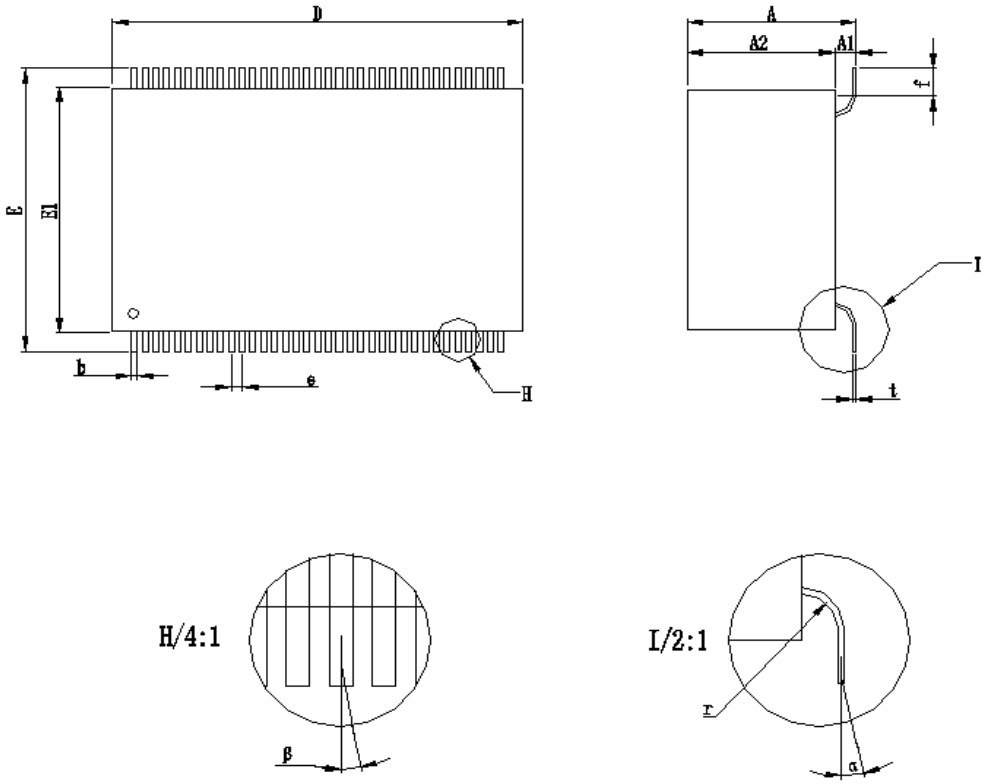


table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD2G40VS70EE5V75	2G	40	-	-	-	SOP70	0 ~ + 70
VDSD2G40VS70IB5V75	2G	40	-	-	-	SOP70	-40 ~ + 85
VDSD2G40RS70SS5V75	2G	40	>50	>80	1	SOP70	-55 ~ + 105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS



	Min	Max
A	10.60	11.30
A2	9.70	10.30
D	23.80	24.20
E	17.40	17.80
E1	14.80	15.20
f	2.00	
b	0.35	
e	0.635	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE：1.U int：mm 2. A1= A - A2		

9 REVISION HISTORY

Table 6 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the Truth Table
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov 10,2017	Add or reduce the chapters