VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD2G32XS70XX4V75 USER MANUAL

Version : B0

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VDIC-SDRAM

HIGH-SPEED 3.3V 64M×32bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

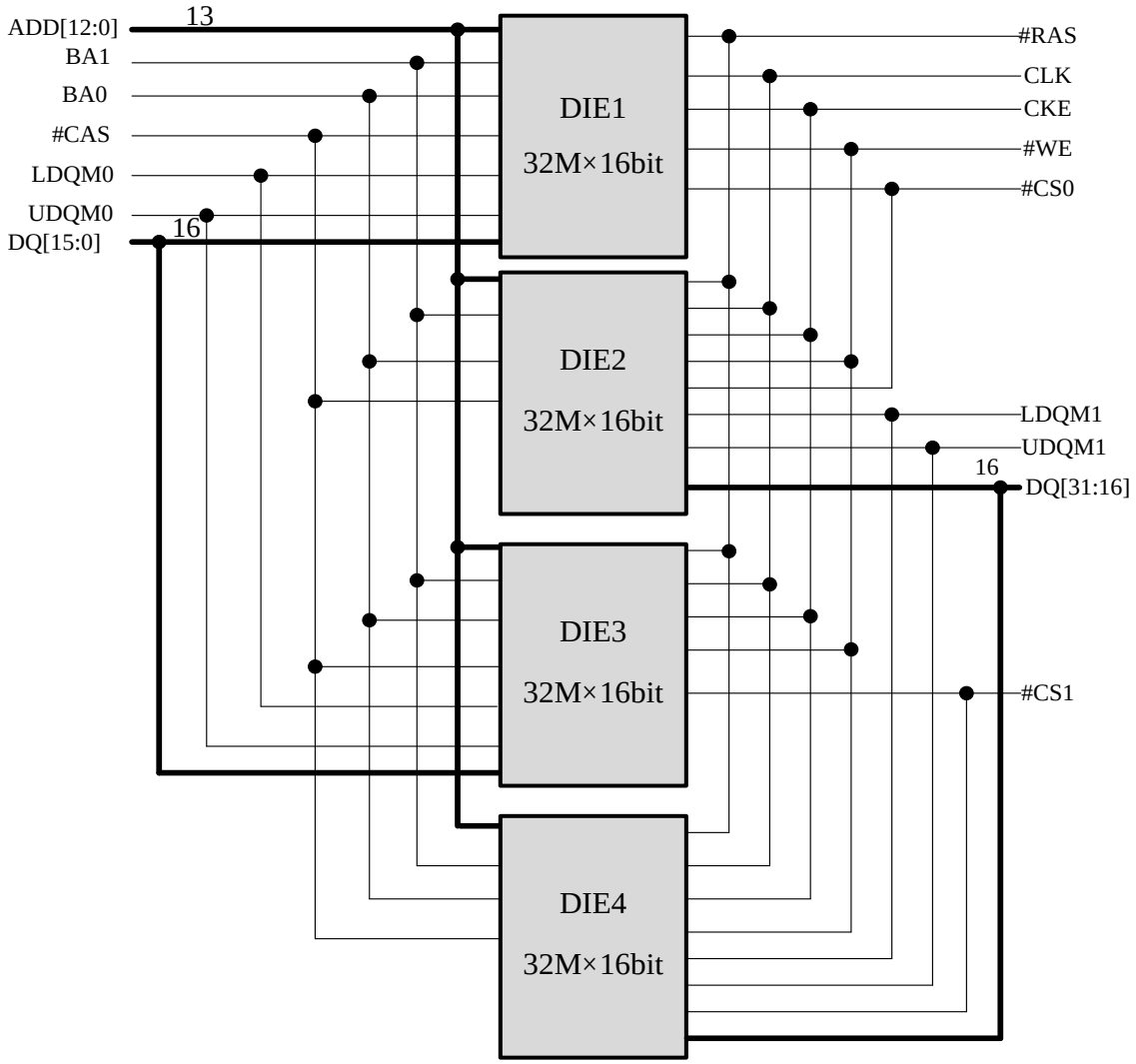
The VDSD2G32XS70XX4V75 is a 2,048M bits SDRAM, organized as 64M words×32 bits. The device has four dies, every die include 8,388,608×16bits×4bank, and a chip select individual. All inputs and outputs are referred to the rising edge of the clock input. Allow the device to be useful for a variety of high bandwidth, high performance memory system applications. It is packaged in 70-pin SOP.

2 FEATURES

- Single 3.3V ±0.3V power supply
- Clock frequency:166,143,133MHz
- LVTTL interface
- Fully synchronous; all signals referenced to a positive clock edge
- Programmable burst length–(1,2,4,8,ful page)
- Programmable burst sequence:Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency (2,3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 70-pin SOP

3 BLOCK DIAGRAM

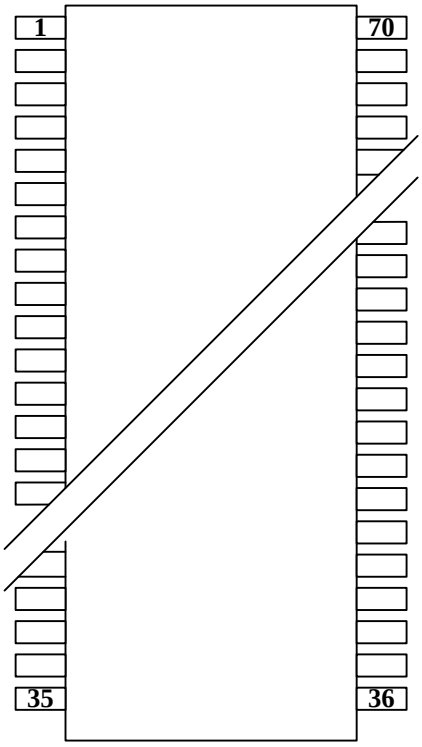
FIGURE 1: Signal link of Block Diagram



4 PIN DESCRIPTIONS

FIGURE3: Pin Descriptions

Pin Id	Pin #		Pin Id
VDD	1	70	**VSS**
DQ0	2	69	**DQ31**
DQ16	3	68	**DQ15**
VDDQ	4	67	**VSSQ**
DQ1	5	66	**DQ30**
DQ17	6	65	**DQ14**
DQ2	7	64	**DQ29**
DQ18	8	63	**DQ13**
VSSQ	9	62	**VDDQ**
DQ3	10	61	**DQ28**
DQ19	11	60	**DQ12**
DQ4	12	59	**DQ27**
DQ20	13	58	**DQ11**
VDDQ	14	57	**VSSQ**
DQ5	15	56	**DQ26**
DQ21	16	55	**DQ10**
DQ6	17	54	**DQ25**
DQ22	18	53	**DQ9**
VSSQ	19	52	**VDDQ**
DQ7	20	51	**DQ24**
DQ23	21	50	**DQ8**
LDQM1	22	49	**UDQM0**
LDQM0	23	48	**UDQM1**
#WE	24	47	**CLK**
#CAS	25	46	**CKE**
#RAS	26	45	**A12**
#CS0	27	44	**A11**
#CS1	28	43	**A9**
BA0	29	42	**A8**
BA1	30	41	**A7**
A10	31	40	**A6**
A0	32	39	**A5**
A1	33	38	**A4**
A2	34	37	**A3**
VDD	35	36	**VSS**



Symbol	Type	Description
A0~A12	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0-DQ31	I/O	Data Input/ Output Ports.
#CS0(Die1/Die2)	Input	Chip select:#CSn enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when #CSn is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while #CSn is HIGH. #CSn provides for external bank selection on systems with multiple banks. #CSn is considered part of the command code.
#CS1(Die3/Die4)	Input	
BA [1:0]	Input	Bank address input(s): BA[1:0] defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
#RAS	Input	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Input	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Input	Write Enable Input. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
LDQM0/UDQM0 LDQM1/UDQM1	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle.LDQM0/UDQM0 corresponds to DQ[7:0] and DQ[15:8], and

Symbol	Type	Description
		LDQM1/UDQM1 corresponds to DQ[23:16] and DQ[31:24]. LDQM0/UDQM0 and LDQM1/UDQM1 are considered as the same state which referenced as DQM.
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
V_{DDQ}	Supply	DQ power: DQ power to the die for improved noise immunity.
V_{SSQ}	Supply	DQ ground: DQ ground to the die for improved noise immunity.
V_{DD}	Supply	Power supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground
NC	-	These should be left unconnected.

5 ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}/ V_{DDQ}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to V_{DD} +0.5	V
Power Dissipation	P_D	1.5	W
Operating Temperature Range	T_{OPR}	-55~ +105	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

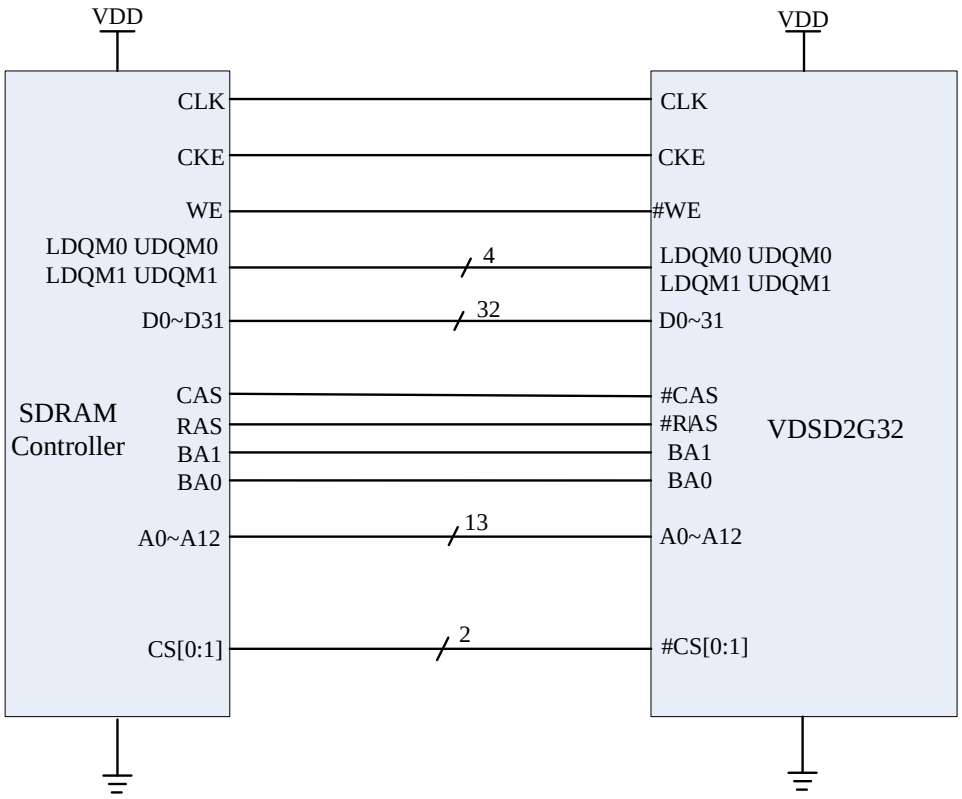
5.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	——	V_{DD}+0.3	V
	V_{IL}	-0.3	——	0.8	V

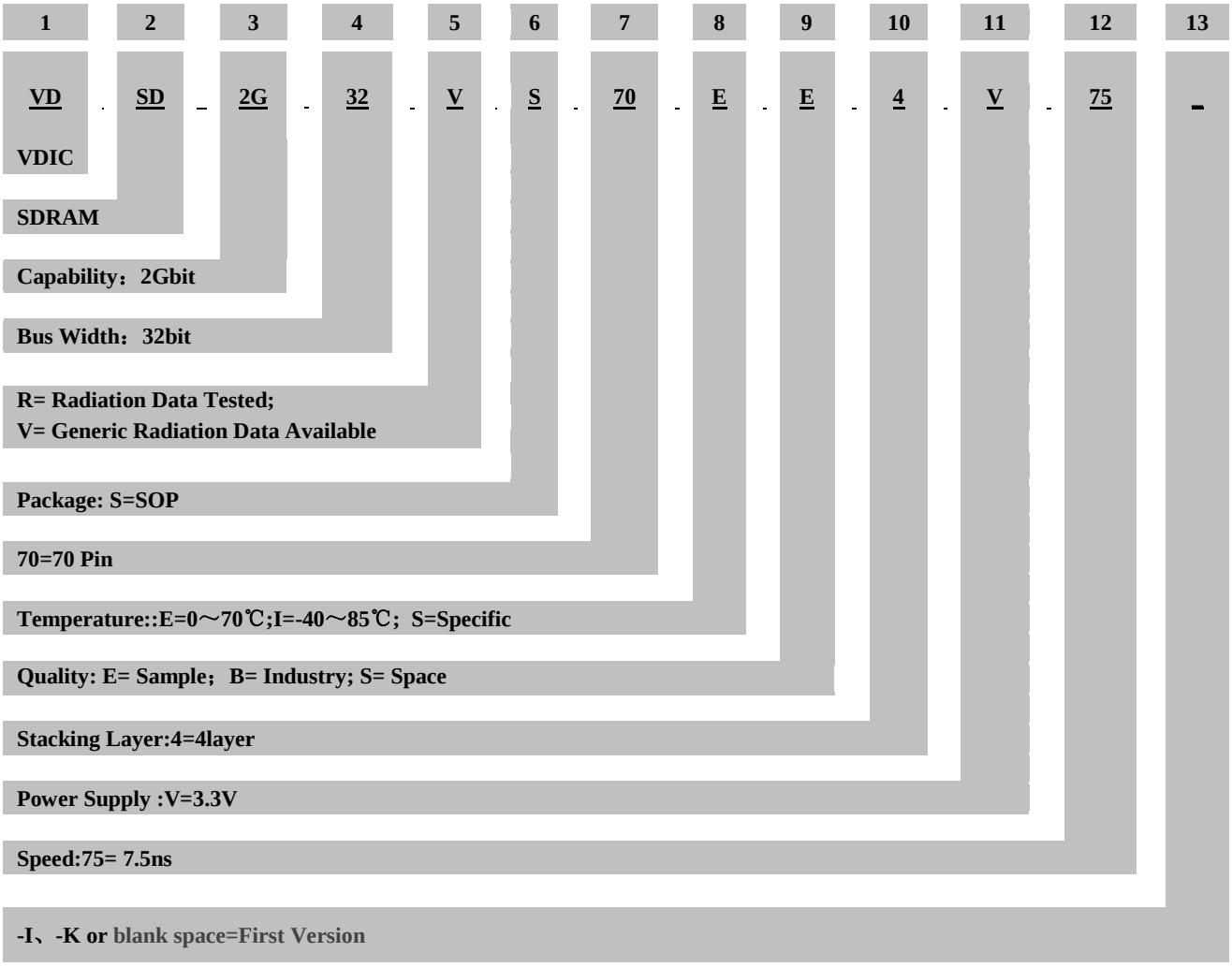
5.3 DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	I_{OL}=2mA	——	0.4	V

6 TYPICAL APPLICATION



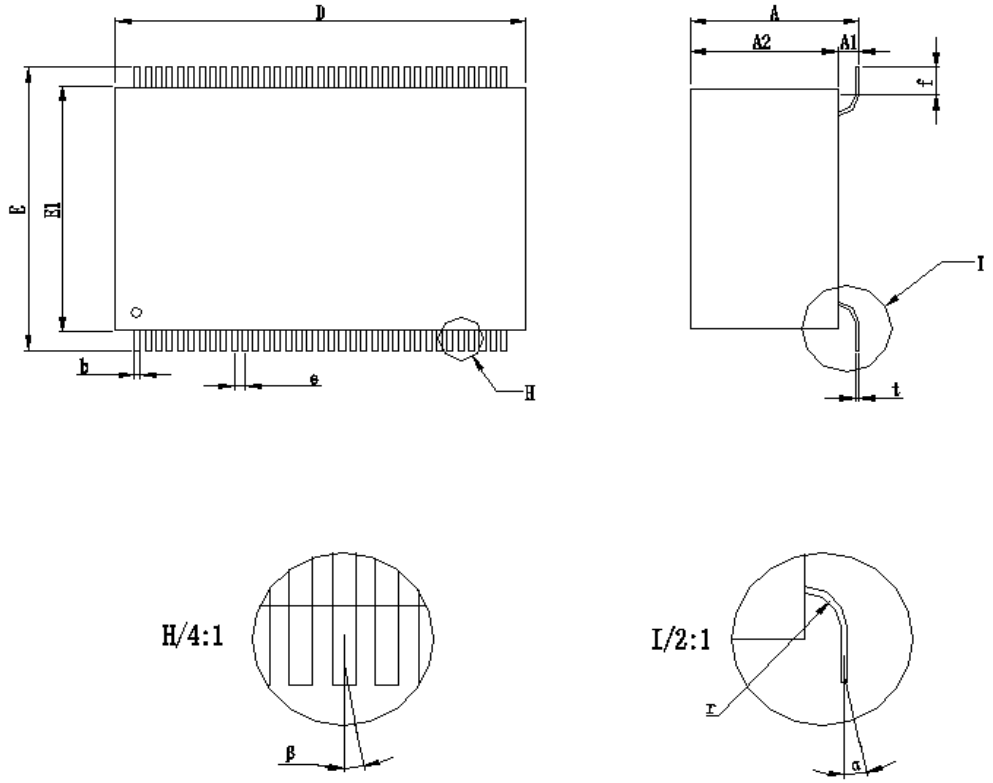
7 ORDERING INFORMATION



Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD2G32VS70EE4V75	2G	32	-	-	-	SOP70	0~+70
VDSD2G32VS70IB4V75	2G	32	-	-	-	SOP70	-40~+85
VDSD2G32RS70SS4V75	2G	32	>50	>80	1	SOP70	-55~+105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS



	Min	Max
A	9.60	10.30
A2	8.40	9.00
D	23.80	24.20
E	17.40	17.80
E1	14.80	15.20
f	2.00	
b	0.35	
e	0.635	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE：1.U int：mm 2. A1= A - A2		

9 REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Aug 23,2016	Modified ORDERING INFORMATION
A3	Jan 9,2017	Modified the Truth Table
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov 10,2017	Add or reduce chapters
B0	Apr 11,2018	Modified DC characteristics table