VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD2G08XS54XX4V75 USER MANUAL

Version : A5

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Zhuhai Orbita Aerospace Science & Technology Co.，Ltd.
Add: Orbita Tech Park，NO.1 Baisha Road，Tangjia Dong ` an，
Zhuhai，*Guangdong,* China 519080
Tel: +86-756-3391979　Fax: +86-756-3391980

Contents

VDIC-SDRAM

HIGH-SPEED 3.3V 256M×8Bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

The VDSD2G08XS54XX4V75 is a 2,048M bits SDRAM, organized as 256M words×8bits. The device has four dies, each die includes 33,554,432 words×4bits×4bank, and a chip select. All inputs and outputs are referred to the rising edge of the clock. The device is useful for a variety of high bandwidth, high performance memory system applications. It is packaged in standard 54-pin SOP (II).

2 FEATURES

- 3.3V power supply
- Clock frequency: 133MHz (max.)
- LVTTL interface
- Single pulsed #RAS
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8, full page
- 2 variations of burst sequence

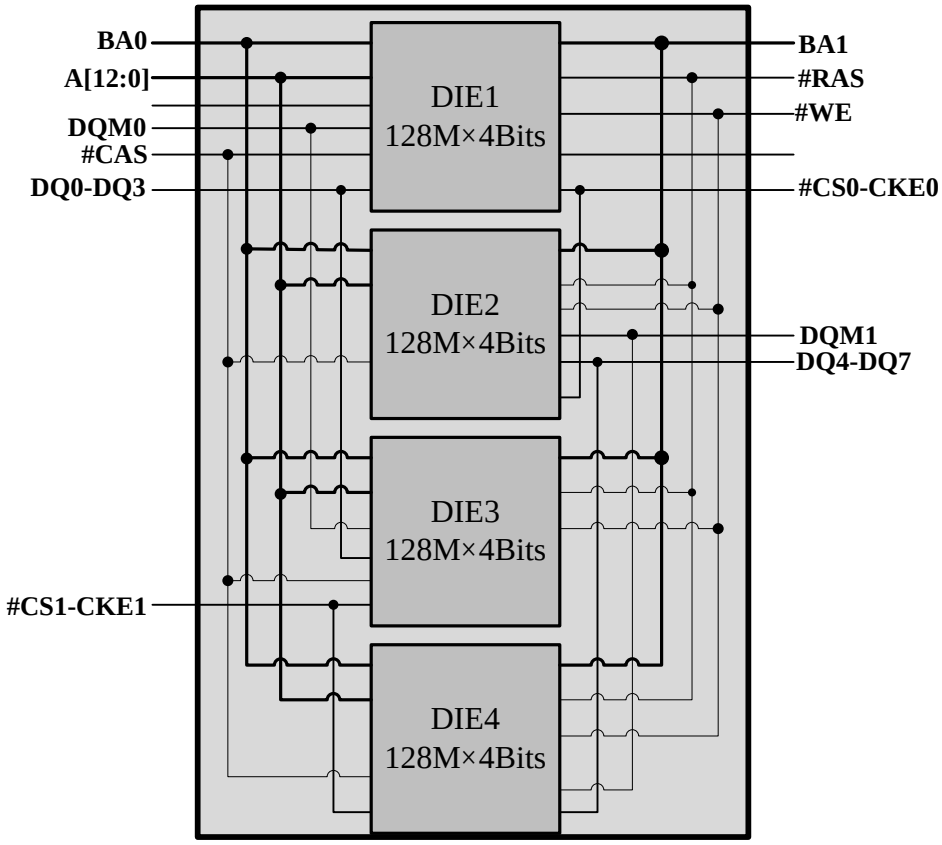
  -Sequential (BL=1, 2, 4, 8, full page)

  -Interleave (BL=1, 2, 4, 8)
- Programmable #CAS latency (CL): 2, 3
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh

  -Auto refresh

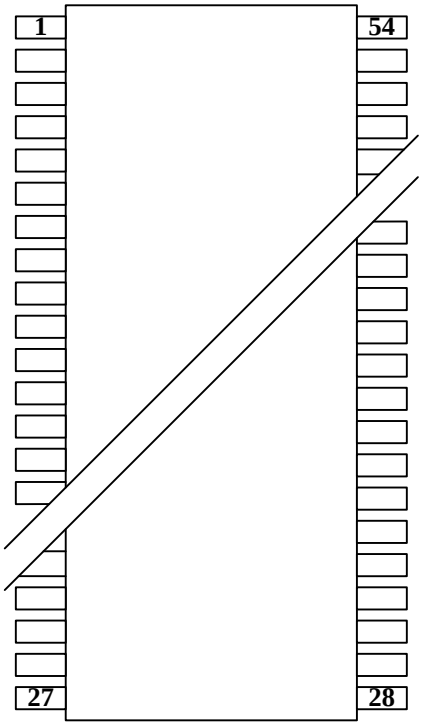
  -Self refresh

3 BLOCK DIAGRAM



4 PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
VDD	1	54	**VSS**
DQ0	2	53	**DQ7**
VDD	3	52	**VSS**
NC	4	51	**NC**
DQ1	5	50	**DQ6**
VSS	6	49	**VDD**
NC	7	48	**NC**
DQ2	8	47	**DQ5**
VDD	9	46	**VSS**
NC	10	45	**NC**
DQ3	11	44	**DQ4**
VSS	12	43	**VDD**
CS1	13	42	**NC**
VDD	14	41	**VSS**
NC	15	40	**NC**
#WE	16	39	**DQM**
#CAS	17	38	**CLK**
#RAS	18	37	**CKE**
#CS0	19	36	**A12**
BA0	20	35	**A11**
BA1	21	34	**A9**
A10	22	33	**A8**
A0	23	32	**A7**
A1	24	31	**A6**
A2	25	30	**A5**
A3	26	29	**A4**
VDD	27	28	**VSS**



Name	Function
A0~A12	Address Input. Row address (AX0 to AX12) is determined by A0 to A12 at the bank active command cycle CLK rising edge. Column address is determined by A0 to A9, A11 or A12 at the read or write command cycle CLK rising edge. And this column address becomes burst access start address.
DQ0-DQ7	Data Input/Output Ports. 8 bi-directional ports are used to read data from or write data into the SDRAM.
#CS0(Die0-Die1)	Die Enable Input .When #CSn is Low, the command input cycle becomes valid. When #CSn is High, all inputs are ignored. However,internal operations (bank active, burst operations, etc.) are held.
#CS1(Die2-Die3)	
BA0,BA1	BA0 and BA1 are bank select signal (BS).

Name	Function
#RAS	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Write Enable Input. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
DQM	DQM controls input/output buffers. Read operation: If DQM is High, the output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. (The latency of DQM during reading is 2 clocks.) Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written. (The latency of DQM during writing is 0 clock.)
CLK	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE	Clock enable.This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down mode, clock suspend mode and self refresh mode.
V_{DD}	Power supply, connect to 3.3V
V_{SS}	Ground
NC	No connect

5 ELECTRICIAL SPECIFICATIONS

- All voltages are referenced to V_{SS} (GND).
- After power up, execute power up sequence and initialization sequence before proper device operation is achieved (refer to the Power-up Sequence).

5.1 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}/ V_{DDQ}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 ~V_{DD}+0.5	V
Power Dissipation	P_D	1.0	W

Characteristics	Symbol	Maximum ratings	Unit
Operating Temperature Range	T_{OPR}	-55 to +105	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

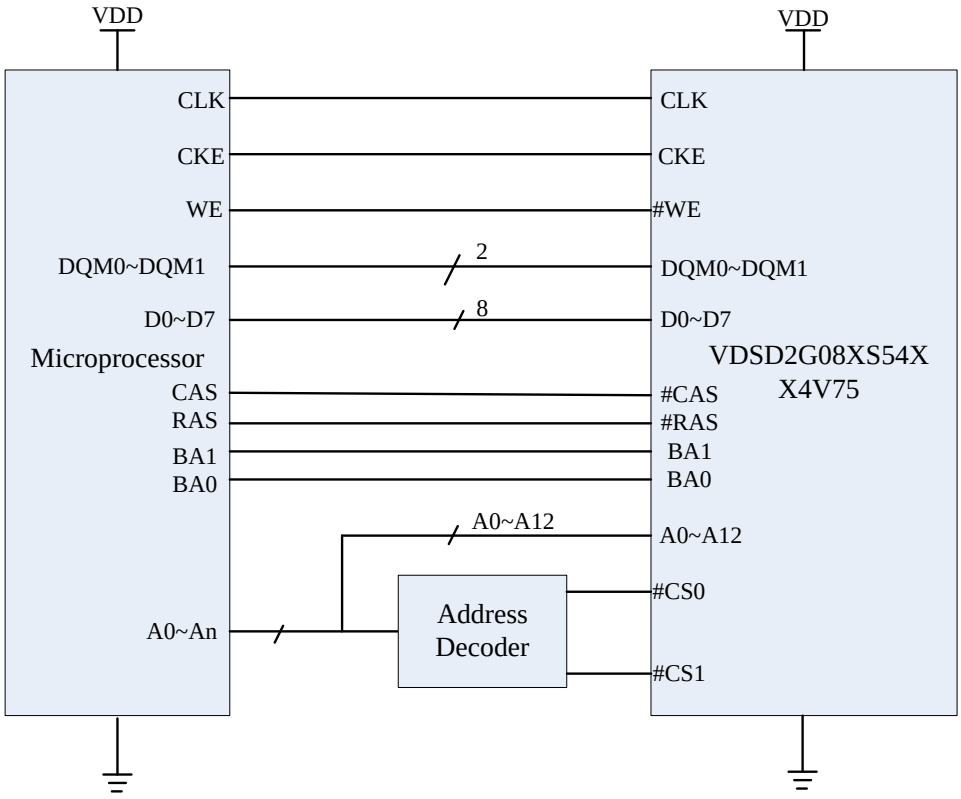
5.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V
	V_{IL}	-0.3	0	0.8	V

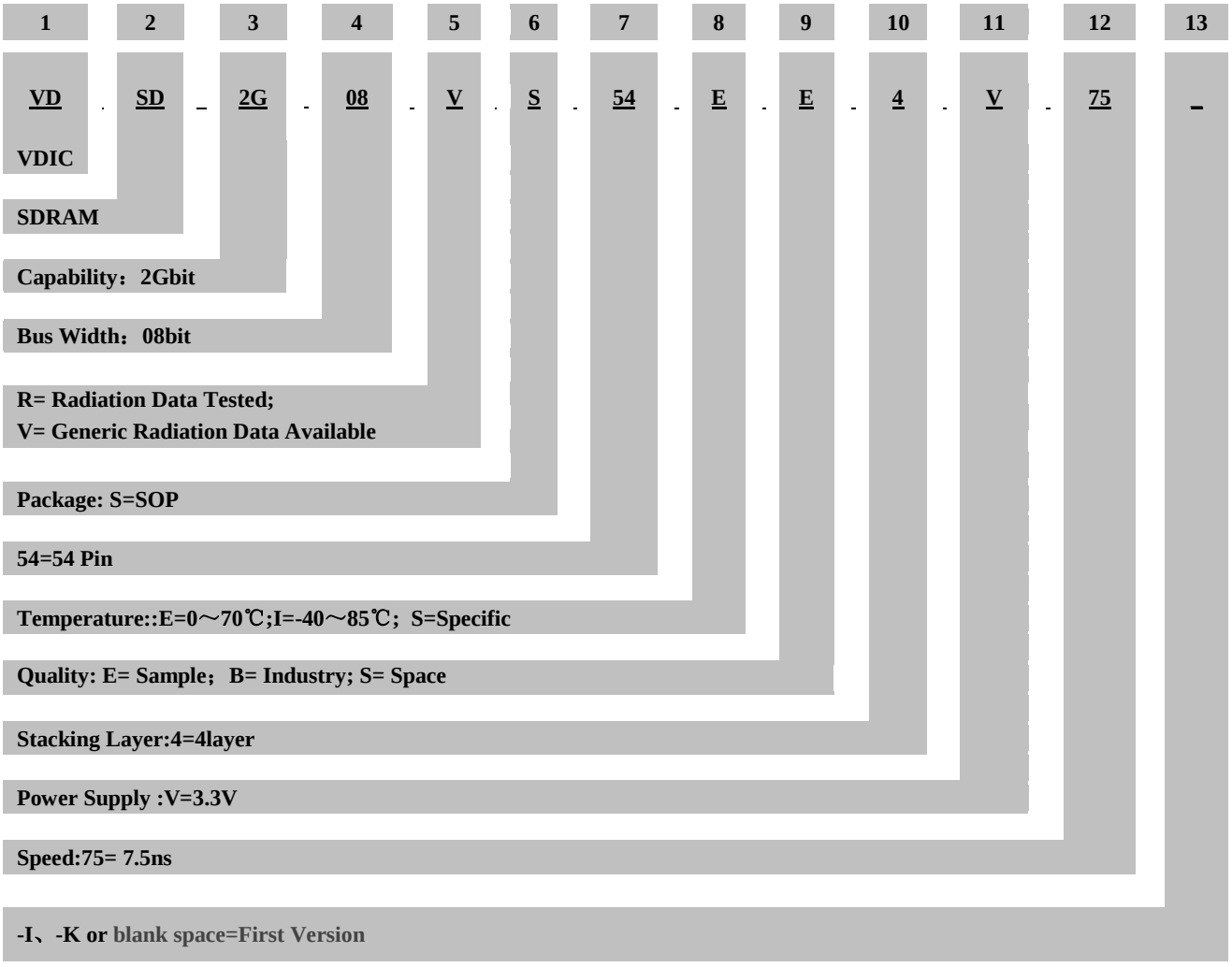
5.3 DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	I_{OL}=-4mA	2.4	——	V
Output Low Voltage Level	V_{OL}	I_{OH}= 4mA	——	0.4	V

6 TYPICAL APPLICATION



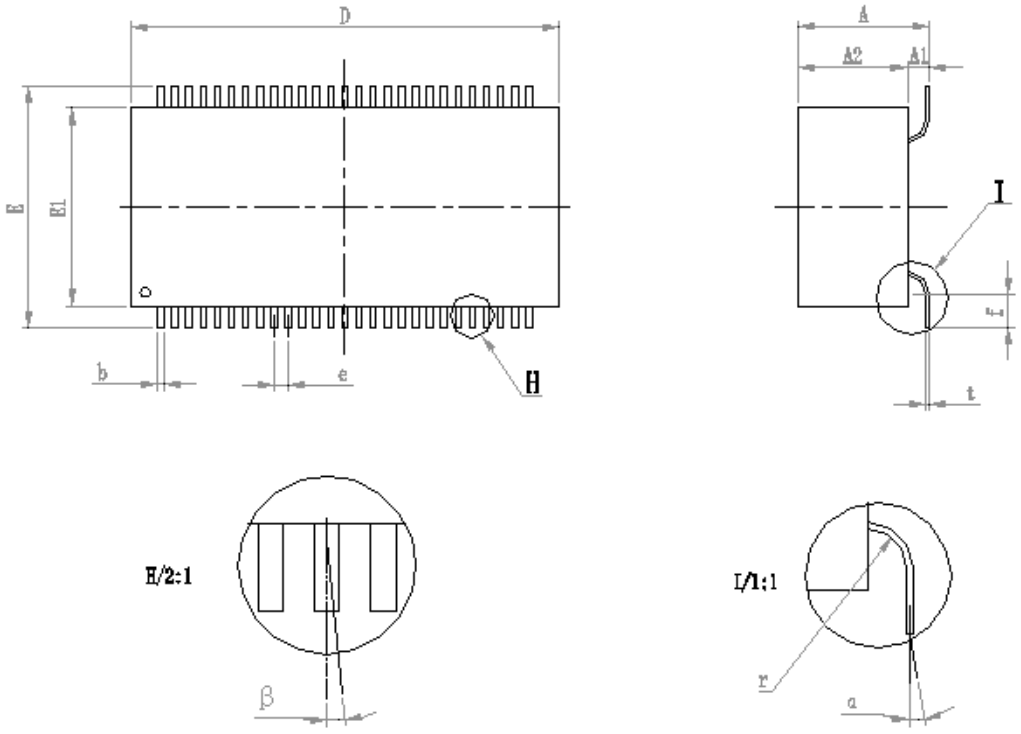
7 ORDERING INFORMATION



Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD2G08VS54EE4V75	2G	8	-	-	-	SOP54	0~+70
VDSD2G08VS54IB4V75	2G	8	-	-	-	SOP54	-40~+85
VDSD2G08RS54SS4V75	2G	8	>50	>80	1	SOP54	-55~+105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS



	Min	Max
A	7.40	7.90
A2	6.20	6.60
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE：1. Unit：mm 2. A1= A - A2		

9 REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Aug 23,2016	Modified ORDERING INFORMATION
A3	Jan 9,2017	Modified the Truth Table
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Apr 11,2018	Add or reduce chapters