

VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD1G16XS58XX2V75 USER MANUAL

Version : A2

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Zhuhai Orbita Aerospace Science & Technology Co. , Ltd.

Add: Orbita Tech Park, NO.1 Baisha Road, Tangjia Dong`an,

Zhuhai, Guangdong, China 519080

Tel: +86-756-3391979 Fax: +86-756-3391980

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VDIC-SDRAM

HIGH-SPEED 3.3V 64M×16bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

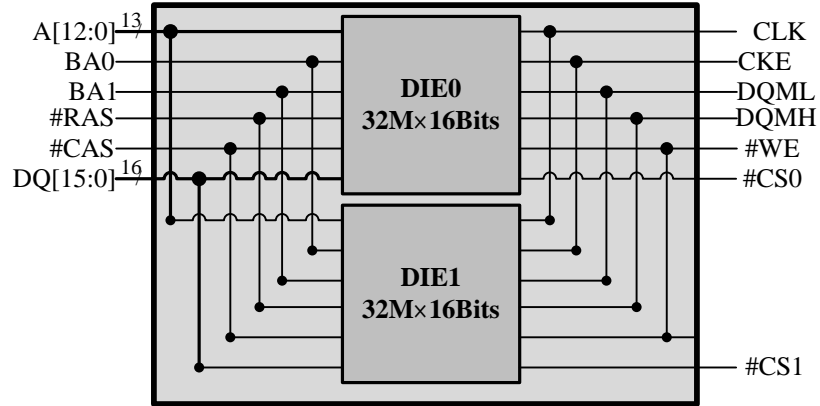
The VDS1G16XS58XX2V75 is a high-speed highly integrated Synchronous Dynamic Random Access Memory containing 1.073.741.824bits, It is organized with two dies of 512Mbits. It is particularly well suited for use in high reliability, high performance and high density system applications, such as solid state mass recorder, serverer workstation. It is packaged in 58-pin SOP.

2 FEATURES

- Single 3.3V ±0.3V power supply
- Clock frequency:166,143,133MHz
- LVTTTL interface
- Fully synchronous; all signals referenced to a positive clock edge
- Programmable burst length –(1,2,4,8,full page)
- Programmable burst sequence:Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency (2,3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 58-pin SOP

3 BLOCK DIAGRAM

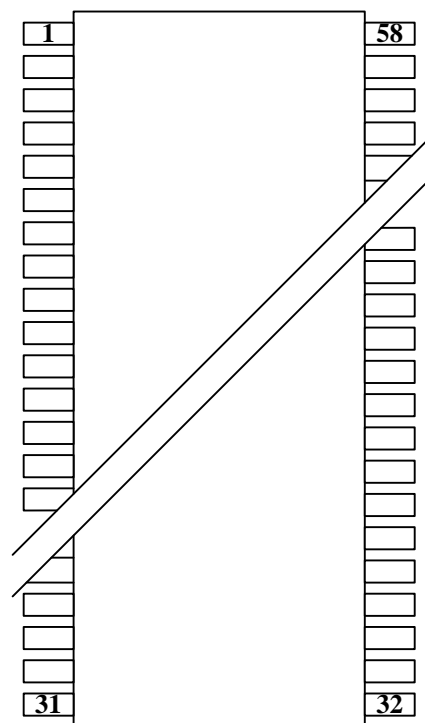
FIGURE 1: Signal link of Block Diagram



4 PIN DESCRIPTIONS

FIGURE 3: Pin Descriptions

Pin Id	Pin #		Pin Id
NC	1	58	NC
VDD	2	57	VSS
DQ0	3	56	DQ15
VDDQ	4	55	VSSQ
DQ1	5	54	DQ14
DQ2	6	53	DQ13
VSSQ	7	52	VDDQ
DQ3	8	51	DQ12
DQ4	9	50	DQ11
VDDQ	10	49	VSSQ
DQ5	11	48	DQ10
DQ6	12	47	DQ9
VSSQ	13	46	VDDQ
DQ7	14	45	DQ8
VDD	15	44	VSS
LDQM	16	43	NC
#WE	17	42	UDQM
#CAS	18	41	CLK
#RAS	19	40	CKE
#CS0	20	39	A12
BA0	21	38	A11
BA1	22	37	A9
A10	23	36	A8
A0	24	35	A7
A1	25	34	A6
A2	26	33	A5
A3	27	32	A4
VDD	28	31	VSS
#CS1	29	30	NC



Name	Function
A0~A12	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a

Name	Function
	LOAD MODE REGISTER command.
DQ0-DQ15	Data Input/ Output Ports. 16 bi-directional ports are used to read data from or write data into the SDRAM.
#CS0 (Die0)	Chip select: #CSn enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when #CSn is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while #CS is HIGH. #CSn provides for external bank selection on systems with multiple banks. #CSn is considered part of the command code.
#CS1 (Die1)	
BA0,BA1	Bank address input(s): BA[1:0] defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
#RAS	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Write Enable Input. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
LDQM, UDQM	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. LDQM corresponds to DQ[7:0], and UDQM corresponds to DQ[15:8]. DQML and DQMH are considered same state when referenced as DQM.
CLK	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst

Name	Function
	counter and controls the output registers.
CKE	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
V _{DDQ}	DQ power: DQ power to the die for improved noise immunity.
V _{SSQ}	DQ ground: DQ ground to the die for improved noise immunity.
V _{DD}	Power supply: +3.3V ±0.3V.
V _{SS}	Ground
NC	No connect

5 ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}/V_{DDQ}	-0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_{IN}	-0.5 to $V_{DD} + 0.5$	V
Power Dissipation	P_D	<2	W
Operating Temperature Range	T_{OPR}	-55~ +105	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

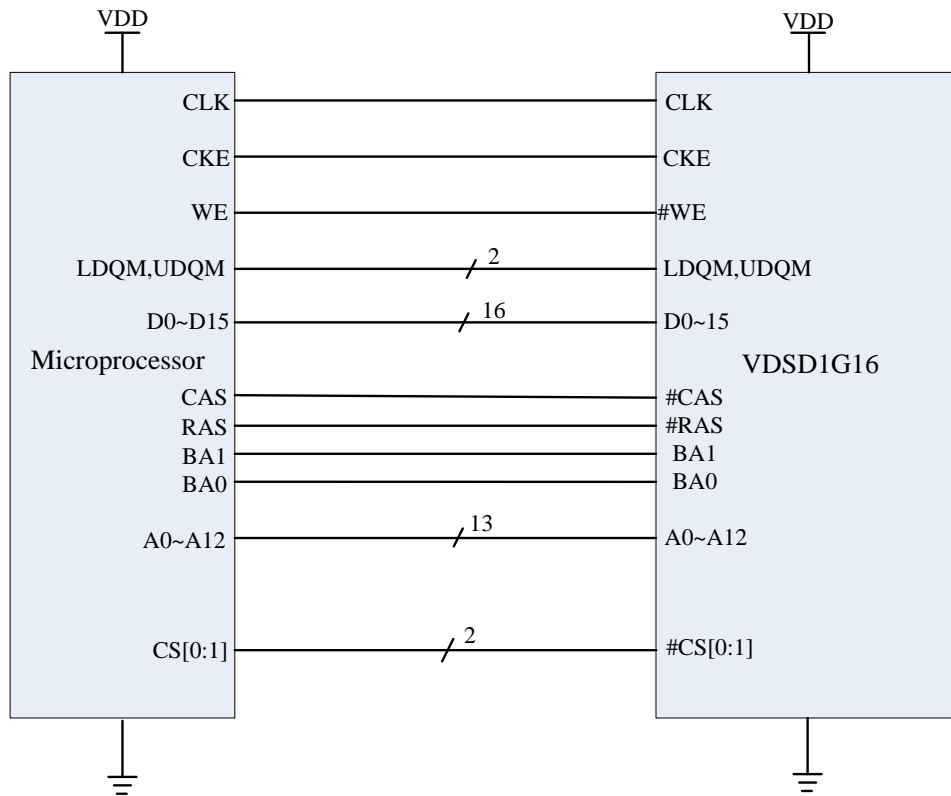
5.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DD}	3.0	3.3	3.6	V
Input voltage	V _{IH}	2.0	—	V _{DD} +0.3	V
	V _{IL}	-0.3	—	0.8	V

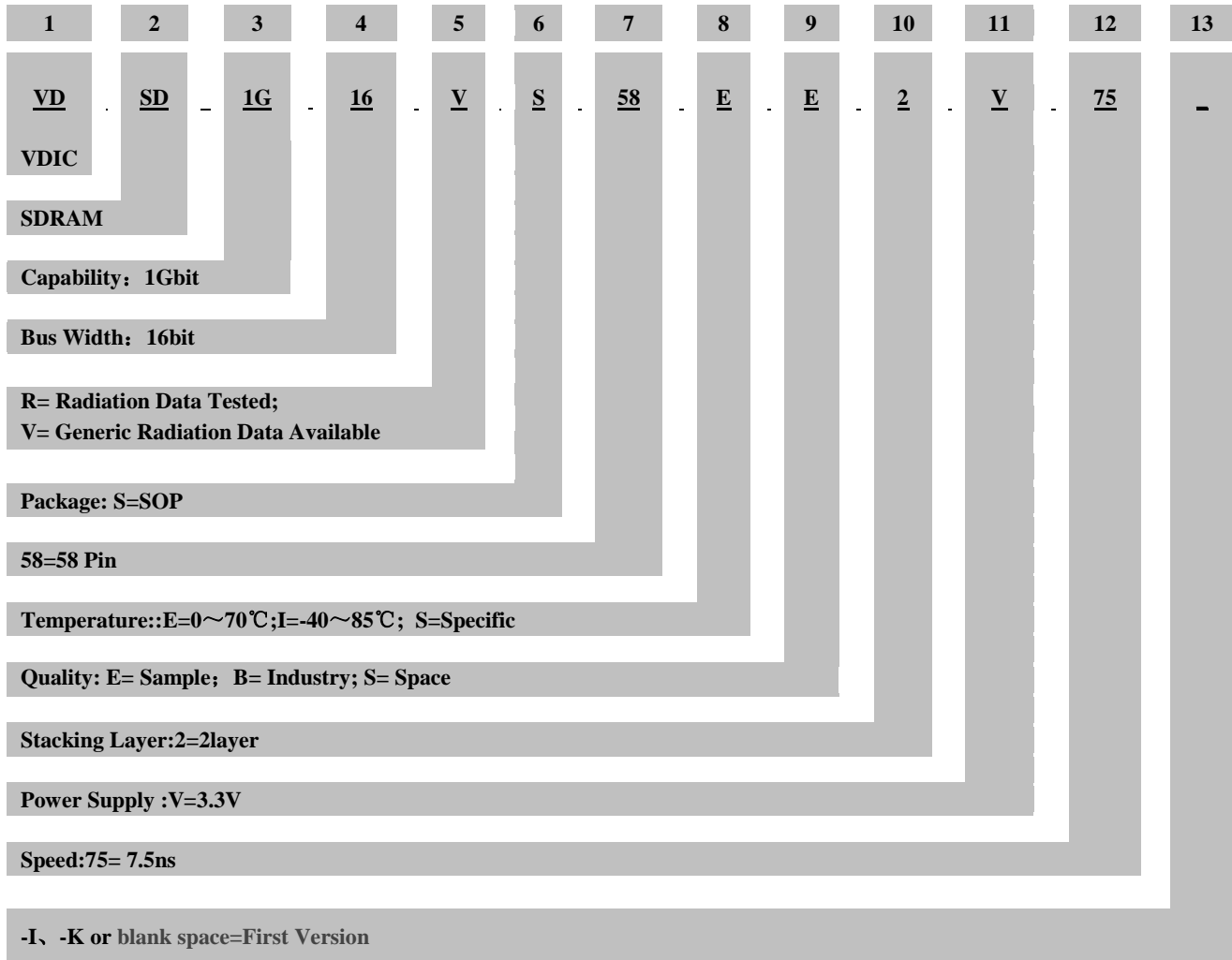
5.3 DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V _{OH}	I _{OH} =-2mA	2.4	—	V
Output Low Voltage Level	V _{OL}	I _{OL} =2mA	—	0.4	V

6 TYPICAL APPLICATION



7 ORDERING INFORMATION



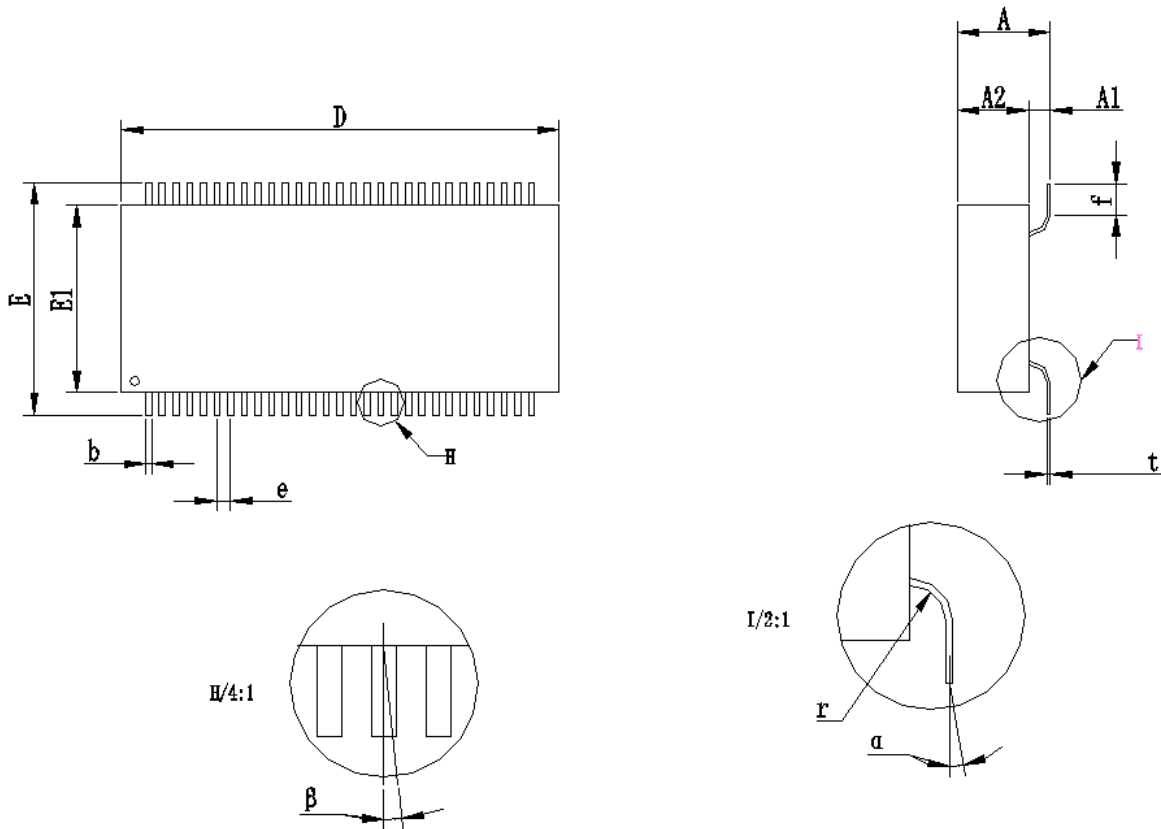
Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDSD1G16VS58EE2V75	1G	16	-	-	-	SOP58	0~+70
VDSD1G16VS58IB2V75	1G	16	-	-	-	SOP58	-40~+85
VDSD1G16RS58SS2V75	1G	16	>50	>80	1	SOP58	-55~+105

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8 PACKAGE DIMENSIONS



	Min	Max
A	5.20	5.70
A2	4.00	4.40
D	25.40	25.80
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	$\leq 3^\circ$	
β	$\leq 3^\circ$	
NOTE: 1.U int: mm		
2. A1= A - A2		

9 REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Apr 11,2018	Reduce chapters