

VDIC SYNCHRONOUS DYNAMIC RAM

VD2D1G08XS74XX1U6 USER MANUAL

Version : A2

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VDIC-DDR2 SDRAM

HIGH-SPEED 1.8V 128M x 8bit

SYNCHRONOUS DYNAMIC RAM

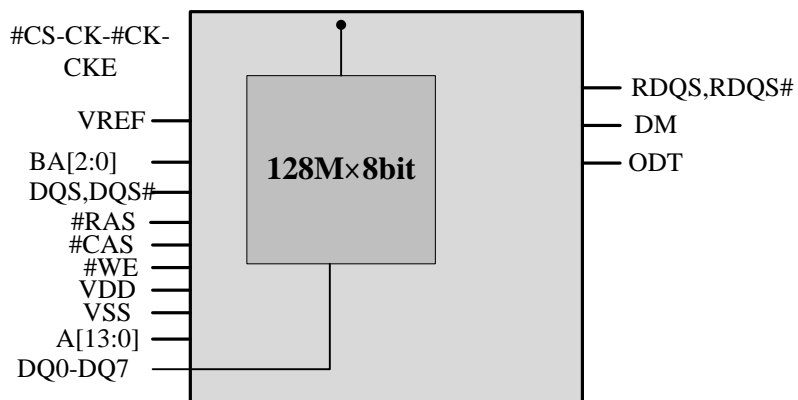
1. DESCRIPTION

The VD2D1G08XS74XX1U6 is a 1024M bits DDR2 SDRAM, organized as 128M words×8 bit. The device has one die, each die includes 1Gbit. The device has a 8-bit interface and is selected with specific #CS, CK , #CK and CKE. The device is useful for a variety of high bandwidth, high performance memory system applications. It is packaged in standard 74-pin SOP.

2. FEATURES

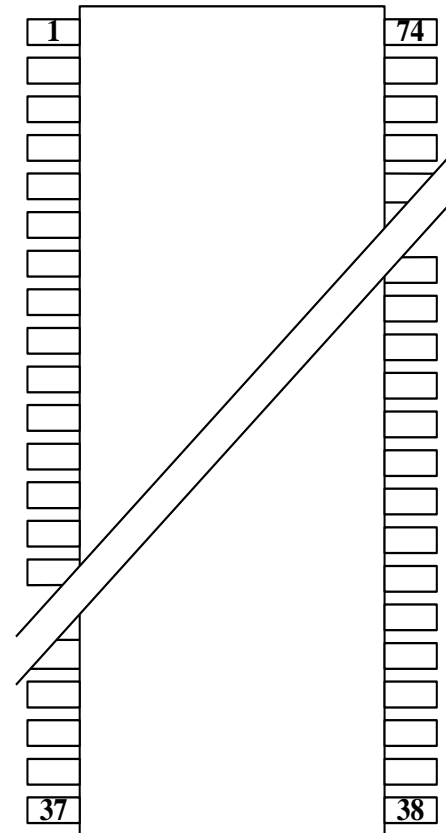
- _Clock frequency up to 400MHz
- _8 internal banks for concurrent operation
- _4-bit prefetch architecture
- _Programmable CAS Latency: 3, 4, 5, 6 and 7
- _Programmable Additive Latency: 0, 1, 2, 3, 4, 5 and 6
- _Write Latency = Read Latency-1
- _Programmable Burst Sequence: Sequential or Interleave
- _Programmable Burst Length: 4 and 8
- _Automatic and Controlled Precharge Command
- _Power Down Mode
- _Auto Refresh and Self Refresh
- _Refresh Interval: 7.8 s (8192 cycles/64 ms)
- _ODT (On-Die Termination)
- _Weak Strength Data-Output Driver Option
- _Bidirectional differential Data Strobe (Single-ended data-strobe is an optional feature)
- _On-Chip DLL aligns DQ and DQs transitions with CK transitions
- _DQS# can be disabled for single-ended data strobe
- _Read Data Strobe supported (x8 only)
- _Differential clock inputs CK and CK#
- _VDD and VDDQ = 1.8V ± 0.1V
- _PASR (Partial Array Self Refresh)
- _SSTL_18 interface
- _tRAS lockout support

3. BLOCK DIAGRAM



4. PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
VSSQ	1	74	VDDQ
RDQS	2	73	DQS
#RDQS	3	72	#DQS
VSS	4	71	NC
DQ6	5	70	DQ7
VDD	6	69	VDD
DQ1	7	68	DQ0
VDDQ	8	67	NC
DQ4	9	66	DQ5
VSS	10	65	VDDQ
DQ3	11	64	DQ2
VSSQ	12	63	VSSDL
VDDL	13	62	NC
VREF	14	61	NC
#WE	15	60	VSSQ
NC	16	59	NC
NC	17	58	NC
NC	18	57	NC
CKE	19	56	NC
#RAS	20	55	NC
BA1	21	54	VSS
BA2	22	53	CK
BA0	23	52	#CK
VDD	24	51	VDD
A10	25	50	NC
A1	26	49	NC
A3	27	48	NC
A5	28	47	ODT
A12	29	46	VSSQ
A7	30	45	A0
A9	31	44	A2
VDDQ	32	43	A4
#CAS	33	42	A6
NC	34	41	A8
NC	35	40	A13
NC	36	39	A11
#CS	37	38	VSS



Symbol	Description
CK, CK#	Input clocks
CKE	Clock enable
CS#	Chip Select
RAS#,CAS#,WE#	Command control inputs
A[12:0]	Address
BA[2:0]	Bank Address
DQ[7:0]	I/O
DQS, DQS#	Data Strobe
RDQS, RDQS#	Redundant Data Strobe
DM	Input data mask
VDD	Supply voltage
VSS	Ground
VDDQ	DQ power supply
VSSQ	DQ ground
VREF	Reference voltage
VDDL	DLL power supply
VSSDL	DLL ground
ODT	On Die Termination Enable
NC	No connect

Note: VDDL and VSSDL are power and ground for the DLL.

5. DC OPERATING CONDITIONS

5.1. ABSOLUTE MAXIMUM DC RATINGS

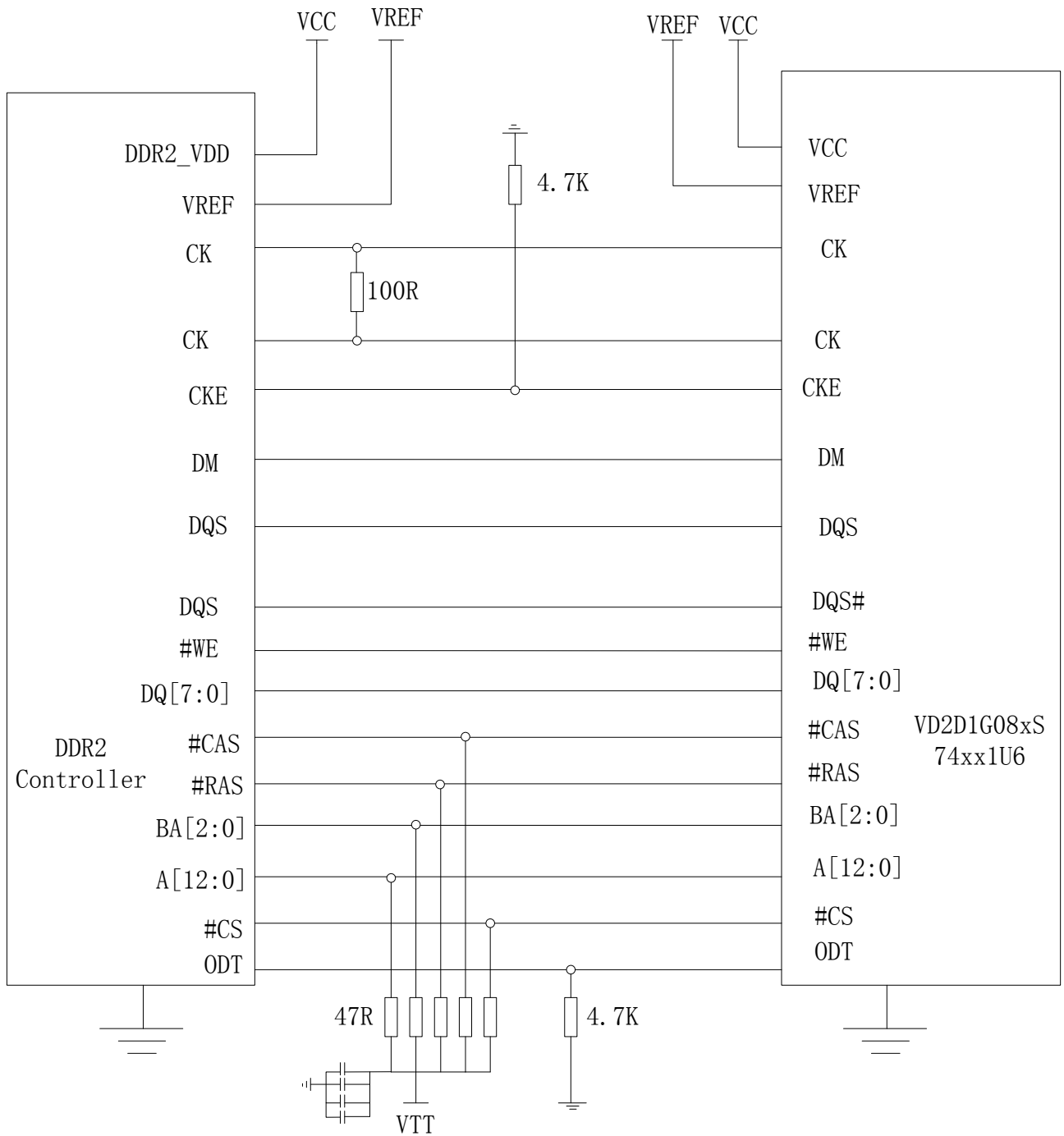
Symbol	Parameter	Rating	Unit
VDD	Voltage on VDD pin relative to Vss	-1.0 to 2.3	V
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 to 2.3	V
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 to 2.3	V
Vin, Vout	Voltage on any pin relative to Vss	- 0.5 to 2.3	V

Symbol	Parameter	Rating	Unit
T _{OPR}	Operating Temperature Range	-55~ +105	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C
I _I	Input Leakage Current	-5 to 5	μA
IOZ	Output Leakage Current	-5 to 5	μA
IVREF	VREF Leakage Current	-2 to 2	μA

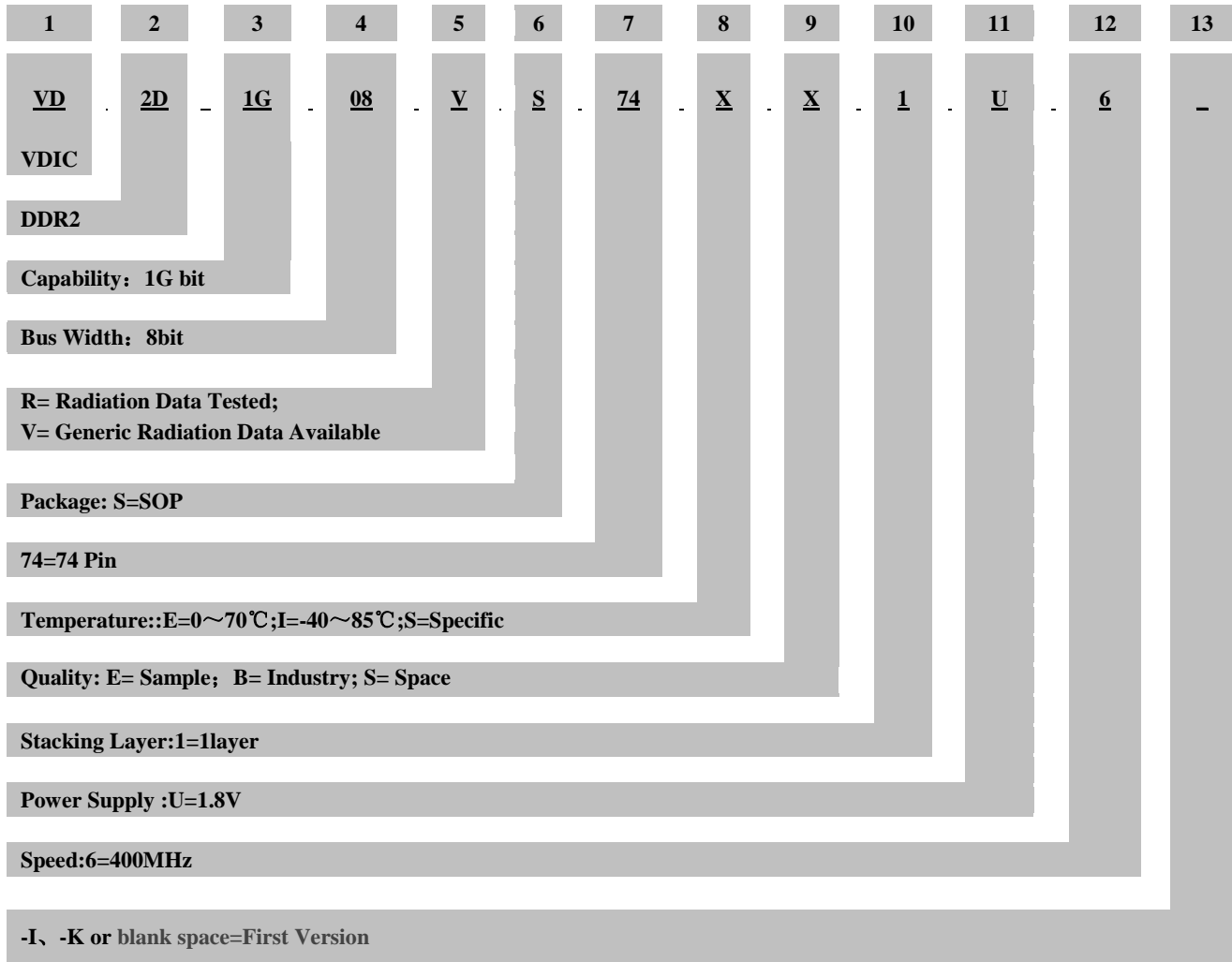
5.2. Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	1.7	1.8	1.9	V
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V

6. TYPICAL APPLICATION



7. ORDERING INFORMATION



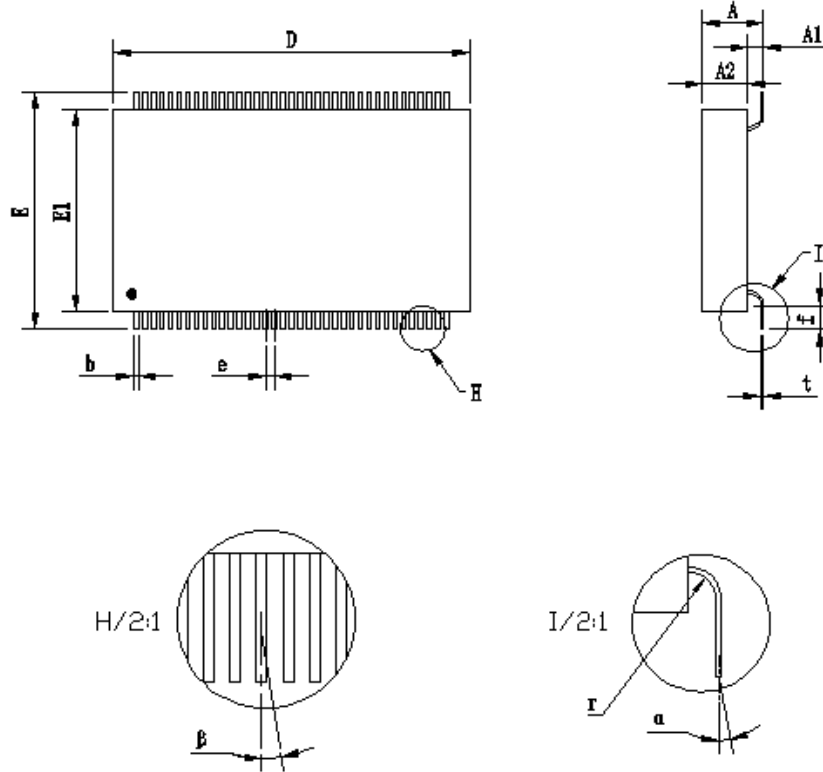
Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VD2D1G08VS74EE1U6	1G	8	-	-	-	SOP74	0 ~ +70
VD2D1G08VS74IB1U6	1G	8	-	-	-	SOP74	-40 ~ +85
VD2D1G08RS74SS1U6	1G	8	100	>68	2.3	SOP74	-55 ~ +105

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8. PACKAGE DIMENSIONS



	Min	Max
A	4.30	5.00
A2	3.10	3.70
D	26.60	27.00
E	17.70	18.10
E1	15.10	15.50
f	1.80	
b	0.35	
e	0.65	
r	1.00	
t	0.20	
alpha	≤3°	
beta	≤3°	
NOTE : 1.U int : mm		
2. A1= A - A2		

9. REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 5,2015	First Created
A1	Mar 21,2016	Modified the PIN DESCRIPTIONS
A2	Mar 15,2018	Add or reduce the chapters.